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# DEVELOPMENT OF A HIGH-VOLTAGE LINEAR ACTUATOR AMPLIFIER SYSTEM

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San Leandro, CA 94577

July 1979

Final Report







AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base, NM 87117

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This technical report has been reviewed and is approved for publication.

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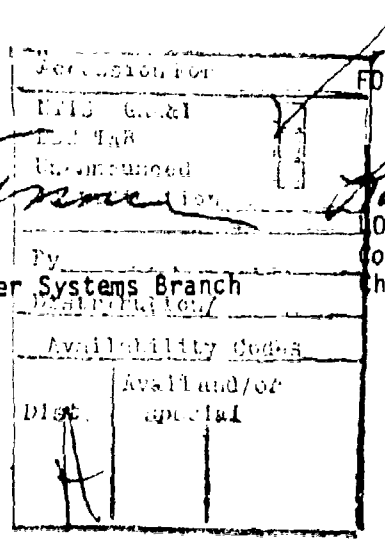


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A lightweight, compact, 61-channel linear switching amplifier system has been developed for aircraft use. Each channel accepts input in the ±10 V range and outputs ±1500 V into a capacitive load of 0.05 μf. The design employs a system of incremental resonant charging of the load, controlled by a system clock. Internal losses are minimized to hold size and weight to a minimum. The amplifiers as designed are flat in frequency response dc to 400 Hz without slew rate limitation. Linearity is better than 1 percent full scale. The

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system is intended to drive piezoelectric actuators of an adaptive optics mirror system. An overall design of the system with computer modeling was completed, and a two-channel breadboard was constructed, debugged, and tested. The tests showed that system design requirements were met with only minor deficiencies in maximum voltage and slew rate, correctable with nominal development efforts.

# CONTENTS

CONTENTS (cont.)

# ILLUSTRATIONS

## ILLUSTRATIONS (cont.)

# LIST OF TABLES

# SECTION 1

## INTRODUCTION AND SUMMARY

Today's laser technology involves high-precision optical elements capable of executing minute deformations, down to a fraction of a wavelength of visible light, in response to realtime signals. The methods of building and using these optical elements has given rise to a whole new technology, adaptive optics. The elements involved are lenses, prisms, and in particular, mirrors.

The mirrors function within the lasers themselves and in the downstream control and application of laser light beams. Laser beams can be focused and aimed by minute deformations or correction locations in the mirror elements. These deformations compensate for atmospheric refraction and defocusing effects. Laser mirrors typically have twenty to seventy deformations or correction locations, the actual number in any one mirror being a compromise between physical size, system requirement, and cost.

Because the motions required of the optical elements are on the order of a few hundred micrometers, the use of piezoelectric (PZ) discs arranged into a stacked configuration ideally suit the requirements. The length of a piezoelectric stack increases with applied voltage, nearly independently of mechanical forces applied to it (except that those forces can also induce voltages in the actuator). A servo command signal can thus be amplified and its output applied directly to the actuator. If the amplifier output is made to be a stiff voltage source (i.e., with constant voltage regardless of current), the amplifier can then absorb the currents induced from mechanical strain on the actuator from any source such as movement of adjacent actuators.

The operational use of PZ transducers in deformable mirrors has been limited by the high-voltage amplifiers required to drive them. Several characteristics of these transducers as electrical loads complicate the design of such an amplifier. The stored electrical energy associated with a given deformation is nearly all of the total energy delivered to achieve the deformation, so the transducers present a nearly pure capacitance to the amplifiers. The output voltage is required to change by a 3000-V swing into a load capacitance of about 0.05 μf, and the bandwidth at this amplitude must be dc to at least several hundred Hz. High-voltage amplifiers previously used in this application have been of class A or AB dissipative designs, typically occupying several equipment racks and weighing several thousand pounds.

The objective of this contract is the development of compact, lightweight, and efficient high-voltage piezoelectric transducer driver amplifiers. The effort covered is the conceptual design of a 61-channel system, and design, fabrication, and testing of a two-channel prototype. Design specifications are presented in Table 1.

The severe volume, weight, and power constraints placed upon the system suggest that a class D switching amplifier be used so that as much energy as possible could be reclaimed and restored during a stack discharge or a down ramp. As opposed to other switching amplifiers, the design developed under this contract uses resonant charging and discharging of the load through an inductor. The resonant circuit is the inductor and the capacitance of the load itself.

## TABLE 1

## SPECIFICATIONS

**The deliverable item includes a two-channel prototype/breadboard of the actuator amplifier system including a common logic breadboard to provide common signals to the channel amplifiers, but does not include dc power supplies.**

| | | |
|---|---|---|
| Power required: | +112 V dc, 2 amp<br>+7 V dc, 0.5 amp<br>-7 V dc, 1 amp<br>+15 V dc, 0.2 amp<br>-15 V dc, 0.2 amp | ±10% |
| | +5 V dc, 0.5 amp<br>-10 V dc, 0.1 amp | ±5% |
| Load Capacitance: | 0.05 µf, ±20% each channel | |
| Gain: | 150 ± 20% adjustable | |
| Offset: | ± 600 V output, adjustable | |
| Linearity: | 1% full scale, including dead band | |
| Input source: | analog signal, operational +10 V to -10 V | |
| Maximum voltage rating on input terminals: | ±40 V | |
| Impedance of input terminals to input signal: | 100 kΩ, except impedance drops to 2 kΩ for input voltages > +10 V and < -10 V | |
| Output voltage range: | + 1500 V to -1500 V | |
| Small-signal frequency response: | dc to 4 kHz (3 db down) | |
| Large-signal frequency response: | dc to 400 Hz (sine wave, slew rate limited) | |
| Slew rate: | 3750 V/ms | |
| Switching clock rate: | 25 kHz, crystal controlled | |
| Switching noise: | dc, 48 db delow full output swing; full amplitude ac, 42 db below full output swing | |
| [illegible] consumption: | up to 120 watts/channel | |

The switching amplifier that has been constructed has very high efficiency and thus can be packaged in a very small volume for the level of energy that it handles. There are no deliberately dissipative elements on the main power flow path; the only losses are the ohmic losses of the inductor and transformer, the ferrite core losses of these components, and the switching losses in the transistors.

Figure 1 is a block diagram of the complete system, showing those sections that must be duplicated 61 times (e.g., the individual channel power stages and associated logic)and those sections that need be present only once (e.g., the common dc power supplies and the common logic). For economy of space and weight, the channel units were packaged in modules of eight. Each module consists of three boards, the logic No. 1 board, the logic No. 2 (piggyback) board, and the main amplifier board--the last carrying the heat sink with its water cooling. Each of these three boards carries its respective part of eight channels.

A detailed description of the final design of the amplifier is given in Section 2. Modifications made to the design during the development and testing program are summarized in Section 3. Actual performance of the amplifier is presented in Section 4, and conclusions and recommendations are in Section 5.

Figure 2 is a photograph of the two-channel prototype and the common logic breadboard.

Results of this program demonstrate that it is feasible to design and fabricate a multi-channel resonantly-charged class D switching amplifier that will meet the essential requirements of

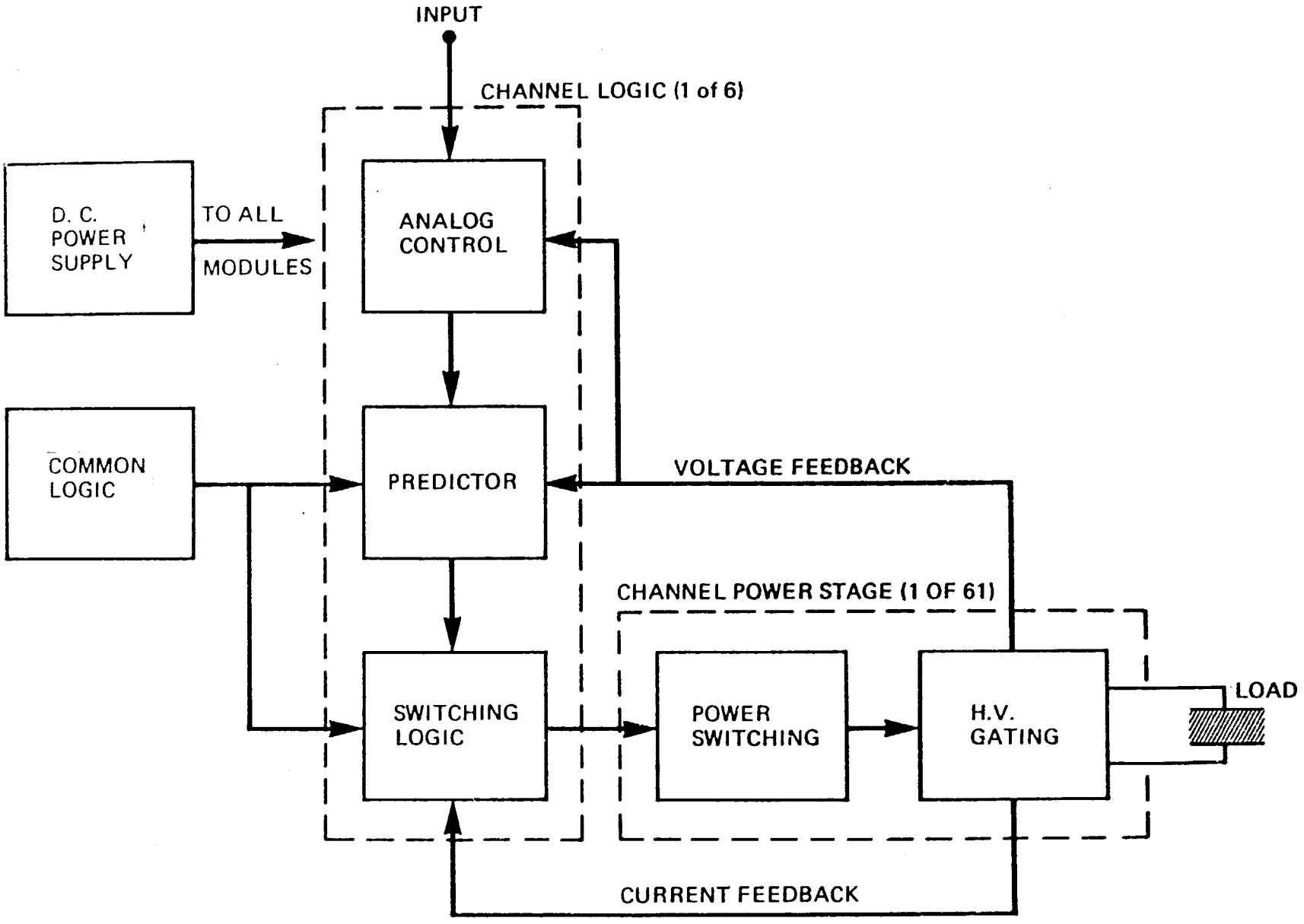



Figure 1. System block diagram.

Figure 2. Photograph of development system.

the specification. The two prototype channels that were developed and tested were shown to operate with no significant crosstalk, and the circuits performed within specifications for drift, linearity, and switching noise.

The system as built meets frequency and dissipation requirements, and at least in design meets voltage and slew rate requirements. Maximum voltage could not be achieved reliably on one of the two channels; above 1350 V, a catastrophic failure would occur, indicative of saturation in the 112-V supply. Volume requirements could not be met without a substantial investment in hybridization, which is out of the question for a proof-of-principle program. The current design requires about a 50 percent increase in weight and volume for the full system; i.e., a full 61-channel system would occupy about 3.0 cubic-feet and weigh about 190 pounds. However, the weight of the coolant is very small, so the weight of the system with coolant is still within 200 pounds.

The worst-case power losses are within specifications. High-frequency (400 Hz), high-amplitude ac is the worst case for power dissipation, and 120 watts/channel is forecast under these conditions.

Although not all the design goals of the project have been achieved, an actuator amplifier system has been designed and a breadboard prototype has shown that the essential design features function. From the advanced base provided by this work, systems with a wide variety of specifications can be designed and built.

# SECTION 2

# SYSTEM DESIGN

## 2.1 INTRODUCTION

This section describes in detail the final design of the amplifier developed under this contract. Schematics of the circuits as built appear in Figures 4 through 9. Modifications made to the initial design during the development and testing program are summarized in Section 3.

The actuator amplifier is a class D, or switching amplifier. Switching amplifiers are inherently more efficient than class A or class B amplifiers, since nondissipative use is made of all components. Like all switching amplifiers, this amplifier is controlled by a system clock, so that at the beginning of each clock period, a comparison is made of the input signal and the voltage on the stack. If the difference exceeds half the "dead band," a switching action is initiated to bring the output to the level commanded by the input. This actuator amplifier has a 25 kHz clock and drives a capacitive load; the switching action results in resonant charging or discharging of the load.

The use of resonant charging is the factor that makes this switching amplifier design different from other class D amplifiers. Since the load is essentially a capacitance, current into or out of it results in a charge voltage across it, rather than in the maintenance of a voltage (as would be the case with a resistive load). Resonant charging of a capacitor, shown in Figure 3a is an inherently nondissipative method of effecting a voltage change

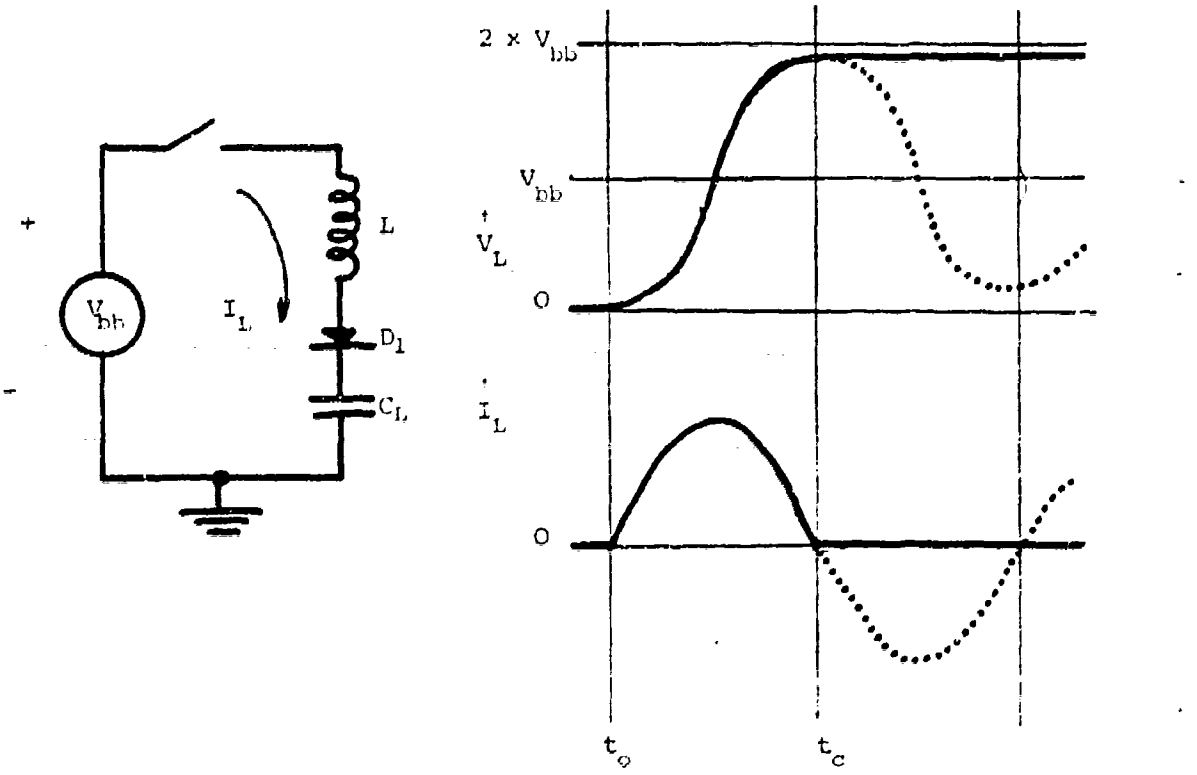



Figure 3a. Resonant charging.

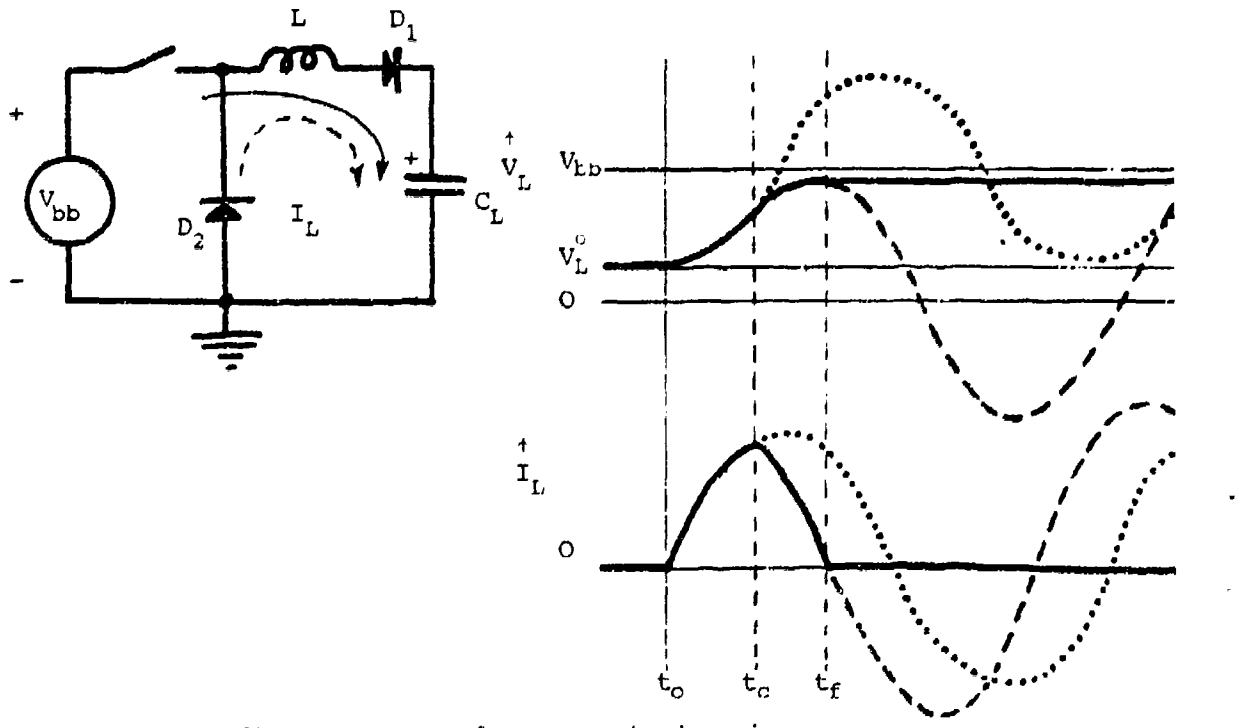



Figure 3b. Incremental resonant charging.

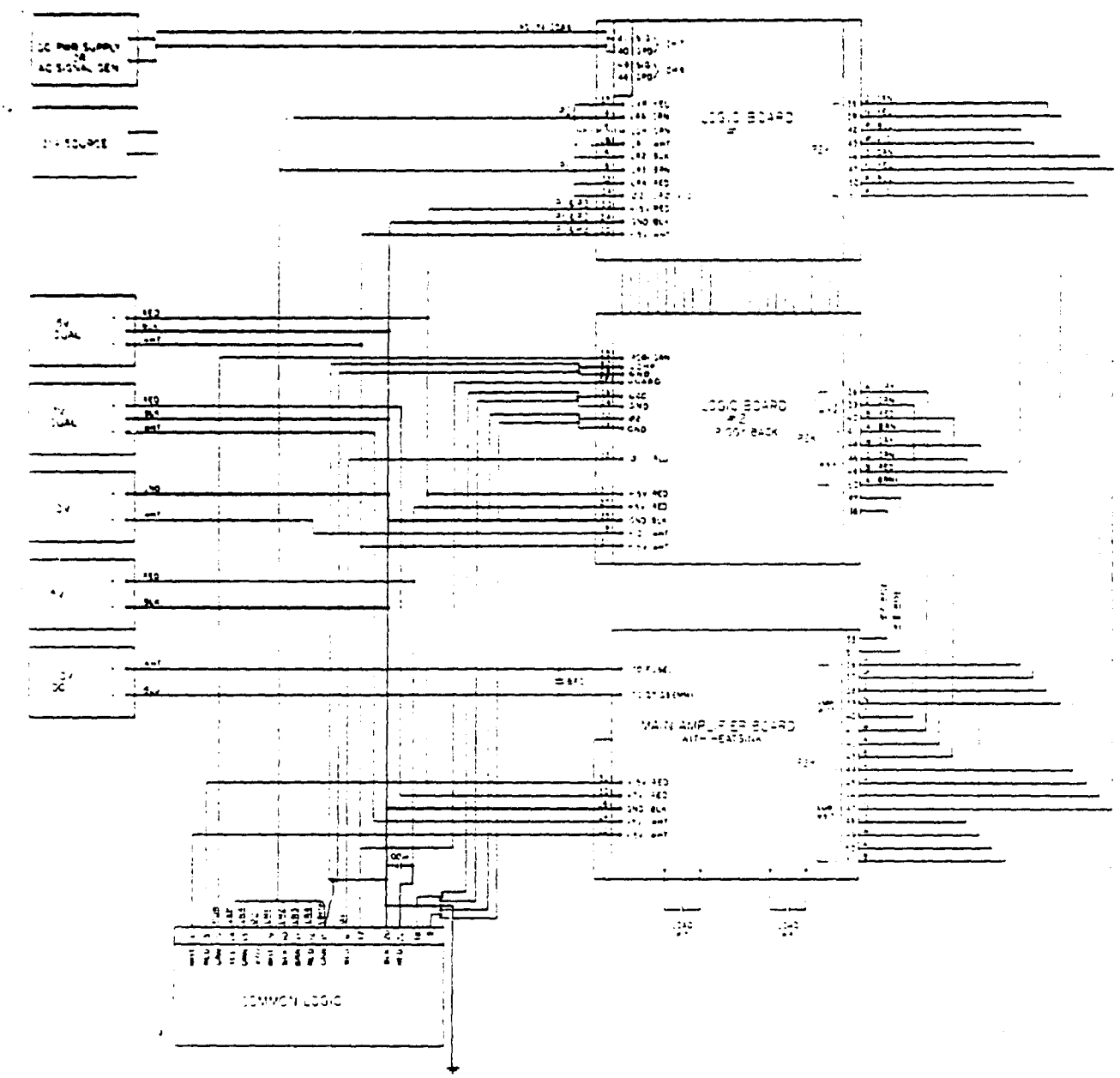


Figure 4. Actuator amplifier prototype and common logic breadboard wiring diagram.

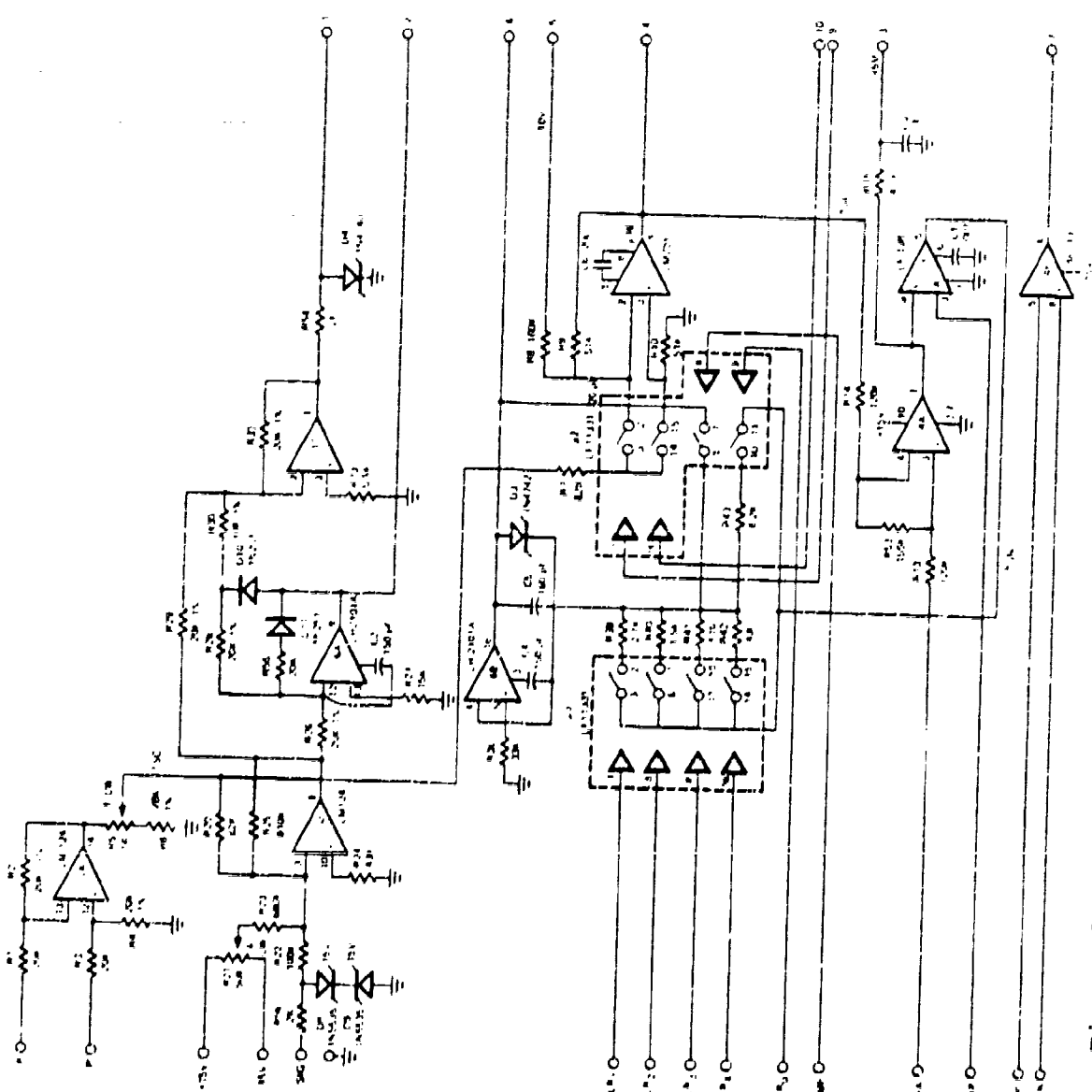


Figure 5. Logic PC board No. 1 schematic.

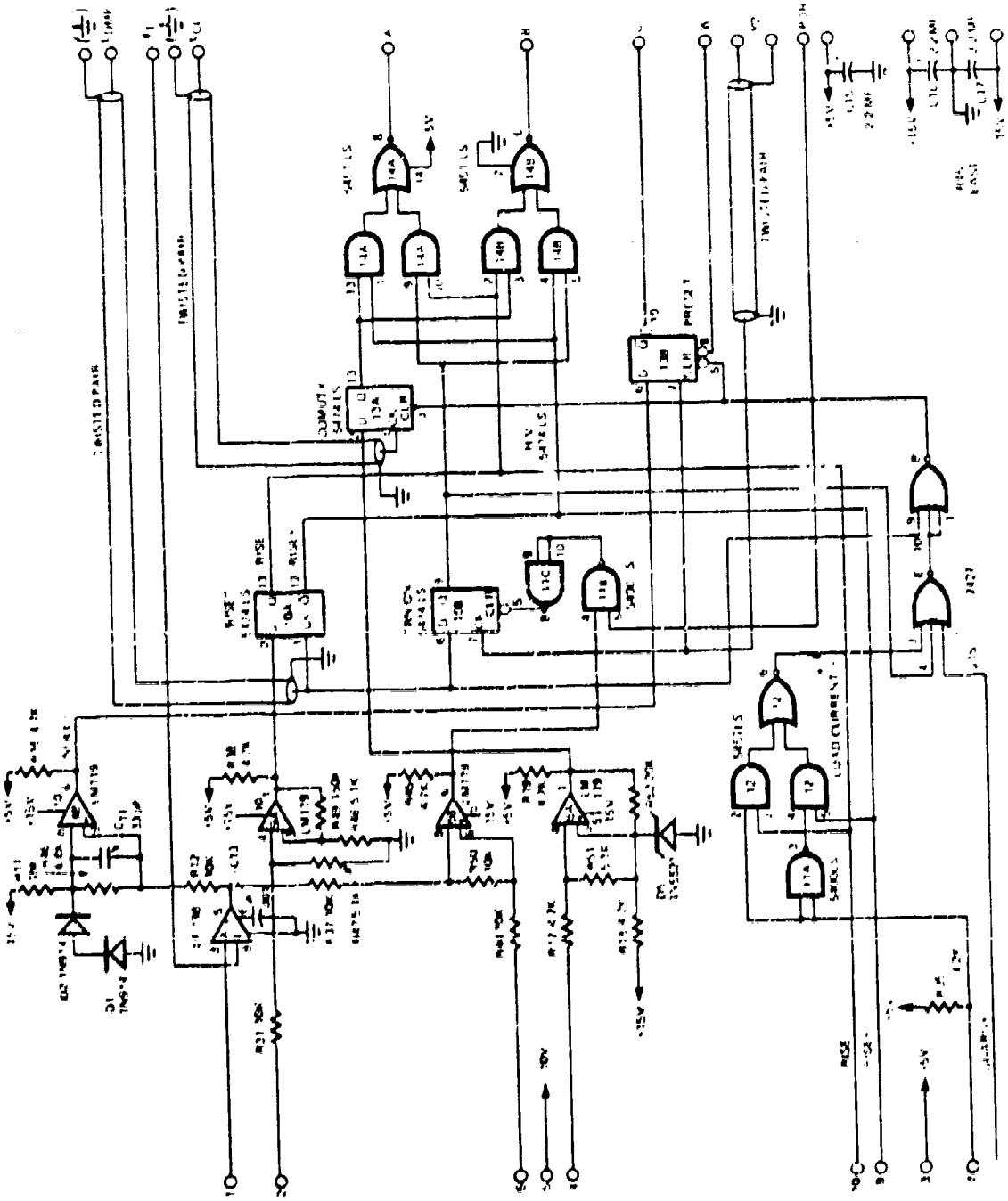


Figure 6. Logic PC board No. 2 (piggyback) schematic.

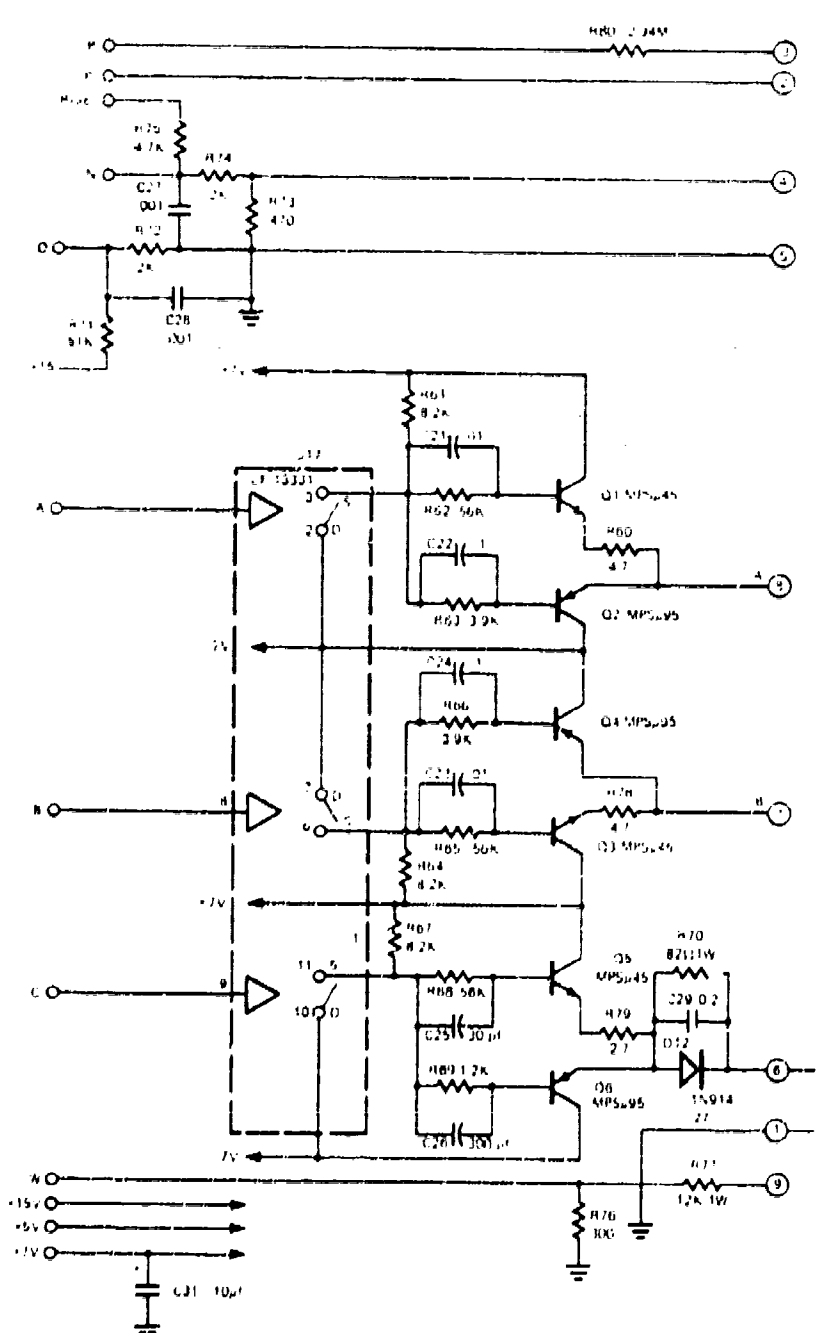


Figure 7. Main PC board schematic (driver circuits).

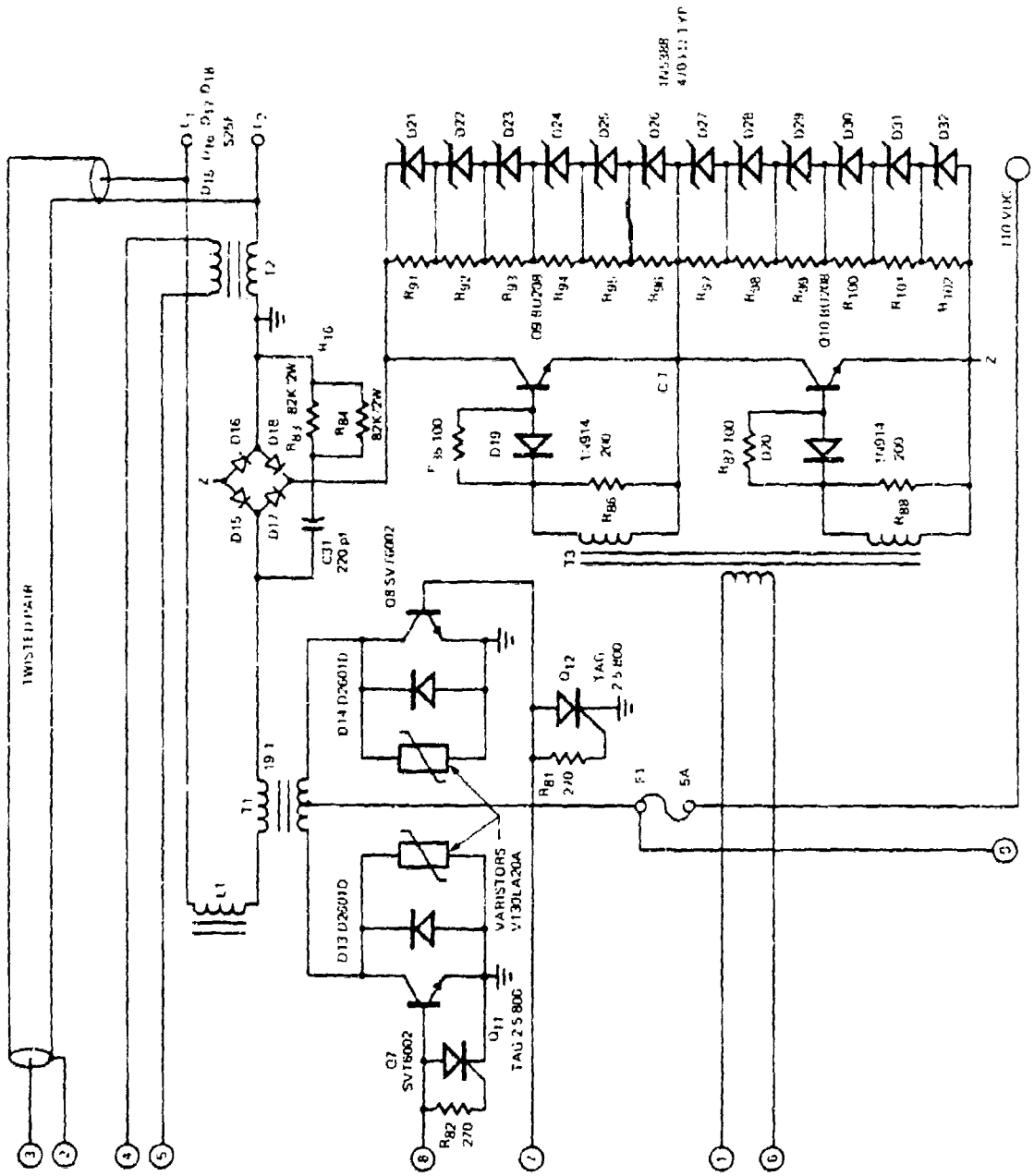



Figure 8. Heat sink schematic.

Figure 9 is a fold-out on page 204 at the back of the report.

to it, as opposed to resistive charging. In this design, incremental resonant charging, illustrated in Figure 3b, is used. The objective illustrated is to raise the output voltage by an amount $\Delta V$. The switch is turned on at time $t_o$; then, at a designated time $t_c$ before $\Delta V$ is attained it is turned off, and the current flowing through it immediately flows (free-wheels) through diode $D_2$. This action reverses the voltage across L, and the current decreases to zero as shown.

The amplifier is dc-coupled, since it is a servo amplifier; it is capable of considerable small-signal frequency response to allow for tight servo lock and for dithering actions. Here, the requirement is a corner frequency of 4 kHz. The large signal frequency response is less than this; it is governed by the slew rate required and in turn by the piezoelectric stack limitation in response to a rapidly changing voltage. This change rate must be held to a level below that which would damage the piezoelectric stack through cracking of the PZ disks or cause instantaneous cavitation by sudden size changes. The amplifier slew rate requirement is set to a value somewhat below this level. For this application, it is 3750 V/ms, or an average current of 0.2 A into and out of the stack.

Within the amplifier's power stage, a dc power source of 112 V has been used, feeding the center tap of transformer $T_1$ (see Figure 8). The switching action takes place on the primary side; the secondary circuit contains the inductor. This arrangement also allows for the output to be bipolar. Since the amplifier is to be dc-coupled, a necessary condition for this type of circuit is that a separate switching means be present in the secondary circuit so that dc voltage can be held off by something other than the magnetizing inductance of the transformer. This condition is provided by two cascaded NPN transistors, $Q_9$ and $Q_{10}$, collectively termed the high-voltage gate (HVG). To allow for bipolar output, these transistors operate through a diode quad ($D_{15}$ through $D_{18}$).

To provide for the 4 kHz bandwidth, a switching clock rate of $2\pi$ times this, or 25 kHz, is selected. To provide the slew rate, the output voltage must be capable of changing up to 150 V in either direction in any one clock period. The slew rate requirement dictates the maximum current occurring in primary and secondary circuits, and the physical size of the major components.

The HVGs are open for a significant period of time within each clock cycle for several reasons. First, the periods of time during which the HVGs are closed with current flowing through them vary with system requirements, whereas the clock periods are fixed; therefore, the longest period of time for which the HVGs could be expected to be closed must be something less than a full clock period. Second, it is necessary for the HVGs to be open for a portion of every cycle so that magnetizing currents in the transformer caused by time integration of dc output voltage will not be cumulative. Third, although efforts have been made to minimize internal capacitances in the inductive elements and, therefore, internal ringing, they cannot be entirely eliminated; time must be provided for the ringing to damp out to avoid its being cumulative. And finally, time is required by the predictive system prior to the start of each active cycle to select the proper curve. Happily, all of these requirements are satisfied concurrently by a single "rest" period in each clock cycle. However, this rest period increases somewhat the maximum peak current that must flow through the inductive elements and the switching transistors.

## 2.2 POWER SWITCHING STAGE

The power switching stage uses resonant charging and discharging of an assumed capacitive load, controlled by incremental timed switching. The charging/discharging inductance $L_1$ (see Figure 8) is set so the resonant charging frequency is one-fourth the clock frequency. For reasons explained above, only one-half

of each 40 μs clock period is available to pass current. In any given clock cycle, a change to the load voltage ranging from a minimum of 10 V (0.6 percent of peak range, within the dead band specification) to a maximum of 150 V (to meet slew rate requirements) may be required. The maximum time for any one charging or free-wheeling current ramp can be expected to be 80 percent of the maximum time available for current to flow, or 16 μs. We wish to make the resonant period much longer than this to linearize the ramps (and thus minimize the maximum current values) while holding the inductance and the air gap size to a reasonable value for linearity of the inductance. An acceptable trade-off is 160 μs for a resonant period. See Figure 16, System Time Line, for an illustration of the relationships of the load voltage, load current, and transistor switching actions.

The high-voltage requirements necessitate use of a transformer, so that the power source and switching transistors operate at a safer, more convenient voltage. For reasons primarily dependent on the ratings of available switching transistors, a supply voltage of 112 V is chosen. Since only NPN transistor types can operate at the necessary voltages and currents with the speed required for a realistic design, a push-pull configuration is used. This configuration causes at least twice the supply voltage to fall across a transistor when it turns off. As a result, the diode at the opposite end of the primary free-wheels the de-popping current; that is, it passes the current generated from the energy stored in the transformer's and $L_1$'s magnetic field. To provide adequate voltage to the inductor, a transformer with an effective turns ratio of 17 to 1 is required. However, because of the masking effects of internal circulating currents caused by various transformer and circuit capacitances, the actual turns ratio required is 19 to 1. The maximum currents in the secondary will be 0.9 A, and in the primary, with magnetizing currents included, 19 A.

Although very close coupling between primary and secondary is not required, close coupling between the two halves of the primary is required, since the transistors along with parallel varistors must depop leakage inductance energy. Also, inter-winding capacitance in the secondary must be minimized, as its value will be multiplied by 361 when referred to the primary, and will form an energy-robbing tank by shunting the magnetizing inductance (see Figure 10). For reasons that will be explained, it is also necessary to minimize the primary-to-secondary capacitance. Furthermore, the magnetizing inductance of the transformer must be closely controlled. The exact value required will be determined by experimentation. The value is fixed by the amount of air gap between the two pot core halves. Too much inductance will result in saturation when there is maximum dc voltage on the output, or when full-amplitude slews are commanded. Too little inductance will result in excessive internal ringing, losses, and leakage inductance, and sensitivity to timing errors.

To maintain a charge on the load between charge cycles, it is necessary to employ switching on the secondary side. NPN transistors that will hold off up to 1500 V are used, and a diode quad is used to allow the load to remain charged in either direction. Although the transistors need not be hot-switched, they must be turned off exactly when the charging current in the secondary drops to zero. Since in practice the turnoff timing is never exact, C1 connected across the quad is provided to absorb any remaining current energy at turnoff, and a resistor is provided to damp out the tank it forms with the charging inductor. The magnetizing inductance of the transformer also provides assistance in desensitizing the system from timing errors.

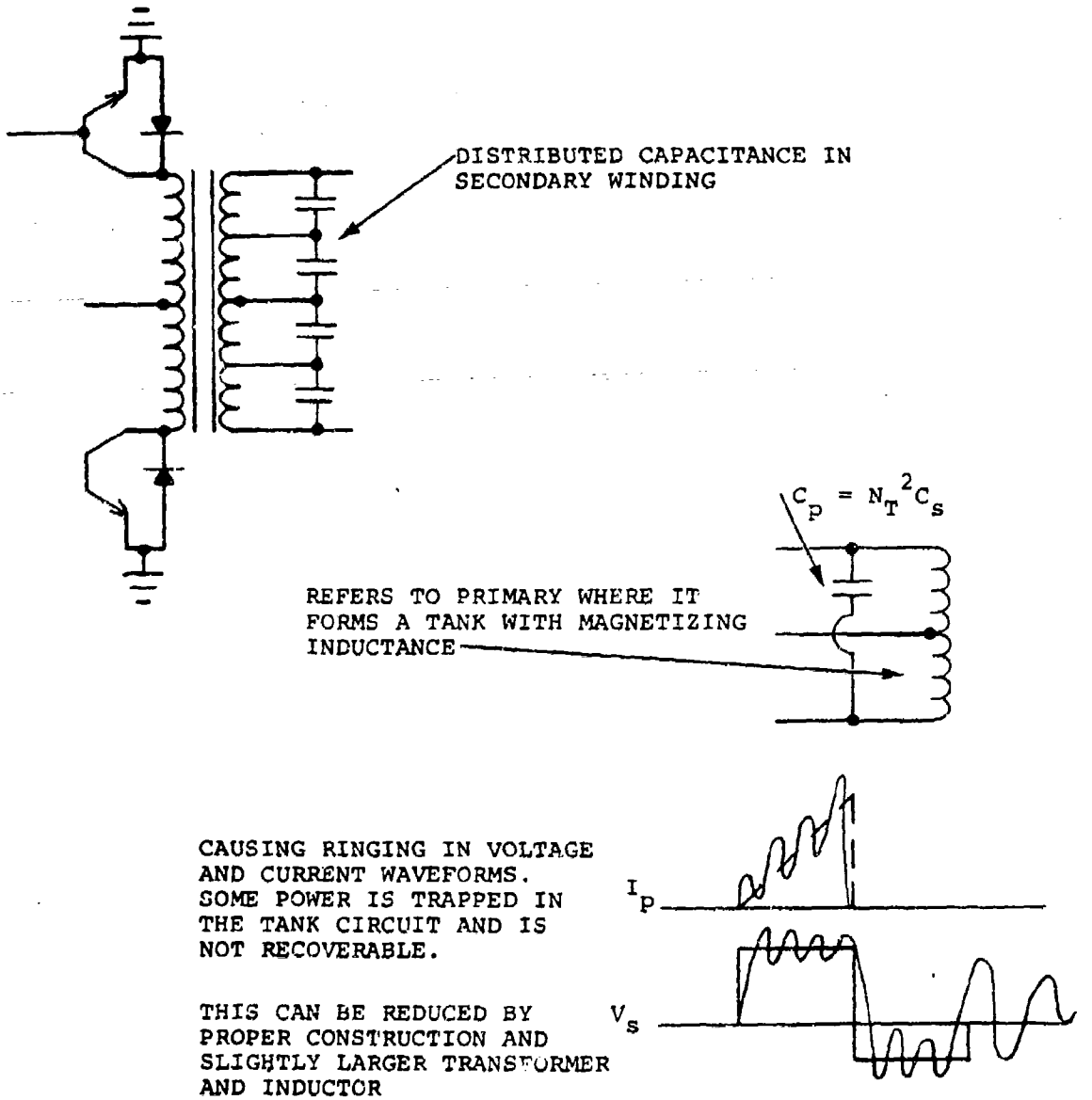


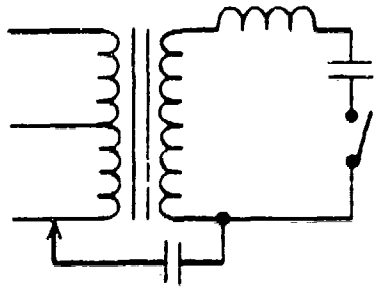

Figure 10, Capacitance problems (transformer).

As a worst case, instantaneous voltages of 3000 V would occur across the switching transistors, because of the voltage doubling action of the transformer interwinding capacitance on the load (Figure 11). The capacitance within the transistors themselves adds to this effect. Since the transistors selected have a hold-off voltage rating of only 1500 V, two transistors in series are provided. In addition, a zener network is provided to dissipate this energy, which would otherwise manifest itself in excessive transistor voltage (Figure 12). The network consists of six 200-V zener diodes in series across each transistor, so that when the total voltage across the two transistors exceeds 2400 V, the zeners conduct; in dissipating power in their avalanche mode, they effectively de-energize the tank created by the magnetizing inductance of $T_i$ and the transistor, and interwinding capacitances.

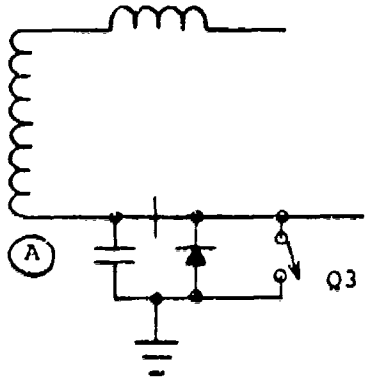
Thus, the power stage of the amplifier is a switching class-D amplifier stage employing a resonant charging both for increasing and decreasing the voltage on the load. In increasing the load voltage, there is a net flow of energy from the capacitance in the 112-V supply to the load (see Figure 13). In decreasing the voltage, there is a net flow of energy from the load to the internal dc supply (Figure 14). The energy is stored internally in large filter capacitors in the 112-volt supply. These capacitors are selected for a total capacitance such that, if all 61 channels are driven in phase with a maximum-amplitude 400-Hz signal, the ripple on the capacitors will be less than 2 percent. A value of 2000 μf is required.

When the load voltage is near zero, the charging and discharging current ramps are of approximately equal duration. When the load voltage is high and the input is commanding it higher,

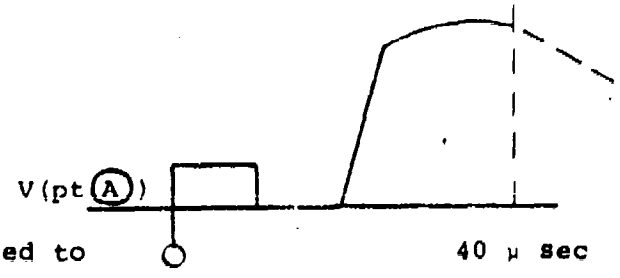
Secondary - Primary
Capacitance - - - -



Point (A) sees capacitance to "ground" which is charged by action of Q3 rectifier quad.



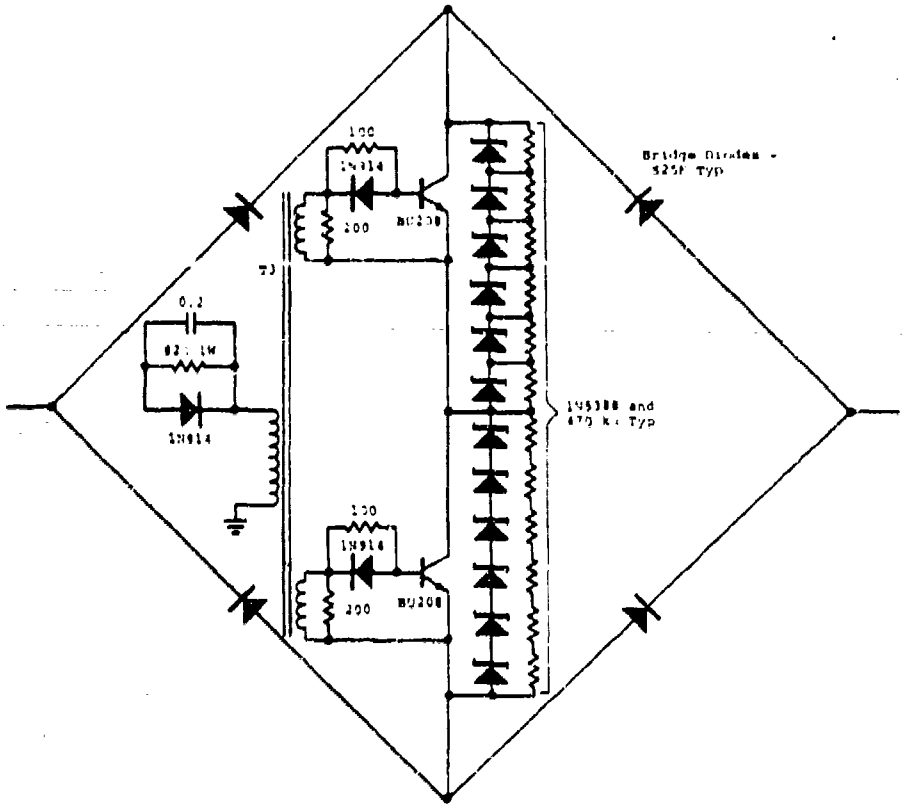

It can discharge only thru magnetizing inductance, or when Q3 turns on during following cycle.
(40 μ sec later)



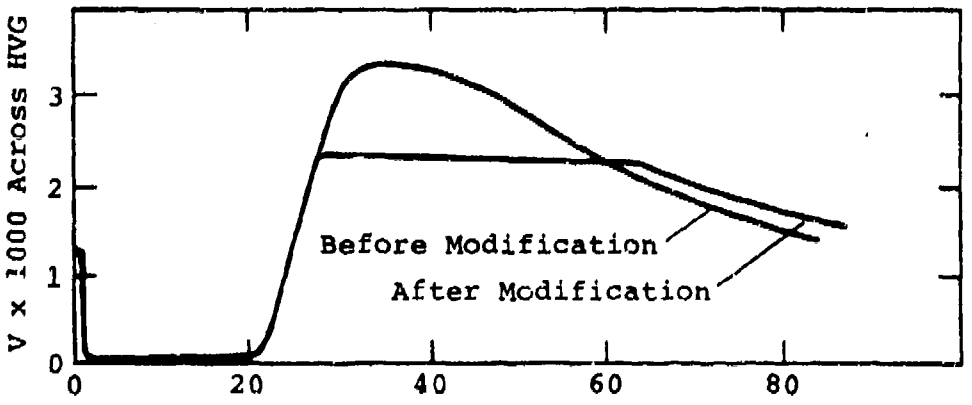

Either way, energy is shunted to this capacitance and lost.

Effective way of solving problem - reduce capacitance by increasing size of transformer.

Figure 11. Capacitance problems (transformer).



a. Zener clamp modification of HVG.




b. Resulting waveforms across HVG.

Figure 12. HVG modification.

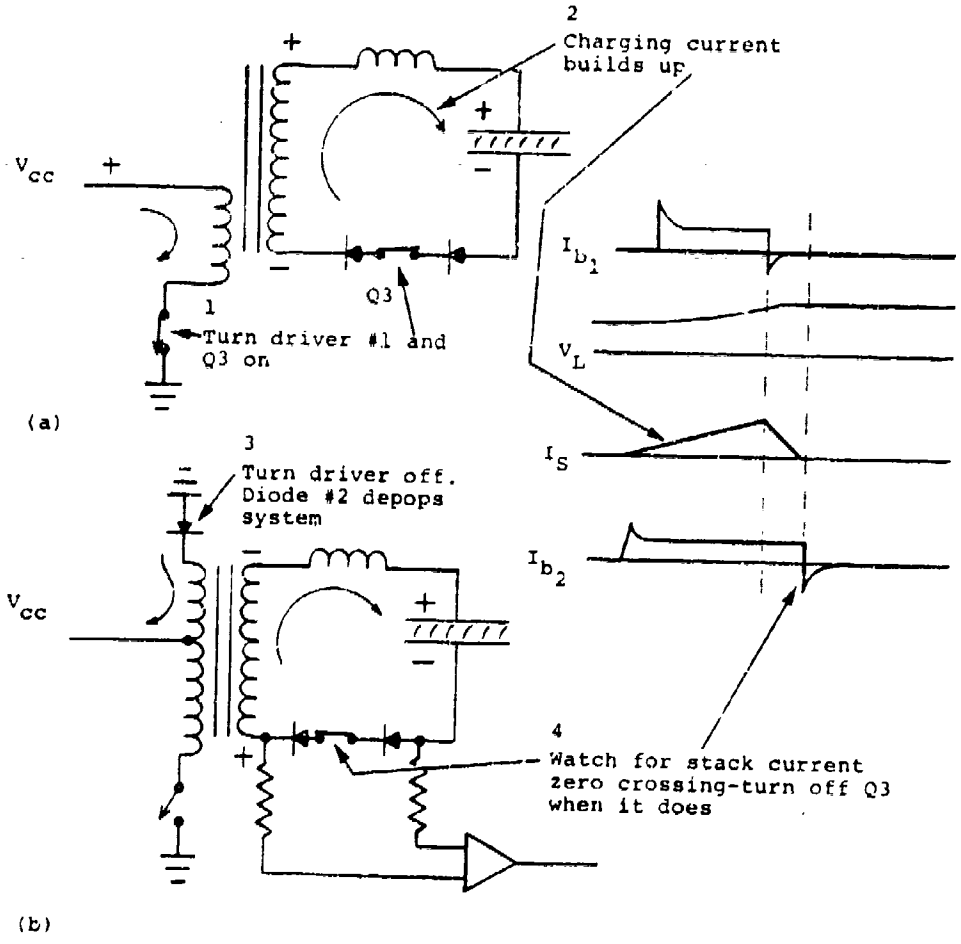



Figure 13. Operation of power switching stage (increasing ramp).

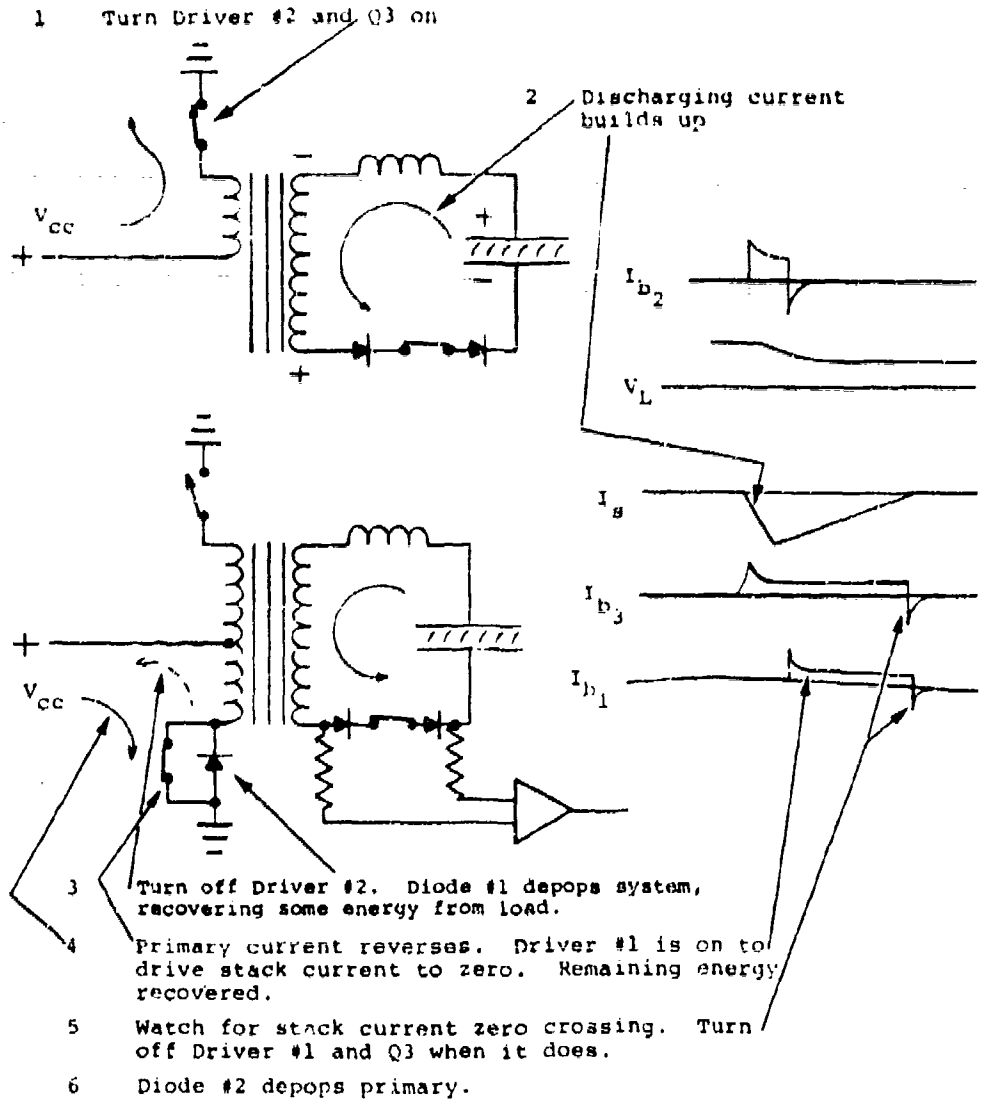



Figure 14. Operation of power switching stage (decreasing ramp).

the charging ramp is longer than the discharging ramp; this difference occurs because the voltage across $L_1$ during the time of the charging ramp is less than during the discharging ramp. Conversely, when the load voltage is high (either positive or negative), and the input is commanding it lower, the charging ramp is short and the discharging ramp is long. In this last case there is an extra commutating cycle applied to the driver transistors. This cycle is necessary because in the decreasing ramp case, the magnetizing current in the transformer crosses zero before the load current does; the extra commutating cycle ensures that negative drive from the primary is applied until the secondary current is forced to zero. Therefore, the drive transistor opposite the one that produces the actual drive is turned on during the free-wheeling period; as the secondary current approaches zero, this transistor begins to conduct primary current in the opposite direction (see Figure 14).

The bases of the driver and high-voltage-output transistors are driven by specially designed base driver circuits to minimize power losses and to obtain minimum turn-off time consistent with secondary breakdown considerations. On each, an NPN Darlington transistor provides the necessary drive to turn on the output transistor; a PN turns it off. These base circuits in essence provide an adequate current source to the base of the appropriate output transistor for turn-on and a stiff -7 volts for turn-off. The circuits were developed during the early stage of the program. Using them with selected PS and HVG transistors, turn-off times considerably better than the manufacturers' specifications were obtained. Turn-off times for the PS transistors (Delco or TRW) of 600 ns were obtained consistently. For the HVG transistors, turn-off times of 1 and 2 μs were repeatedly obtained.

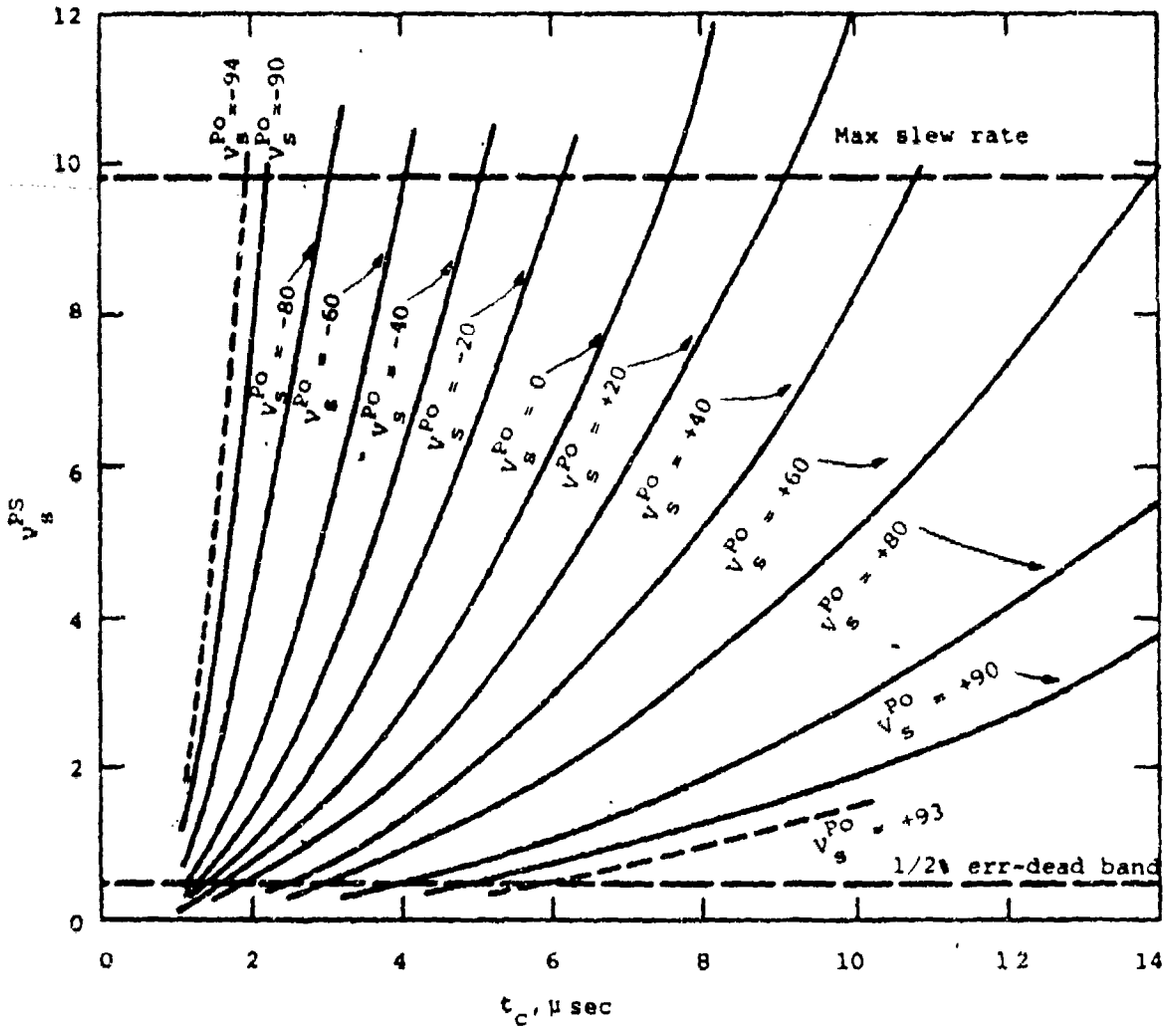
Ideally, there would be no need to power the stack under steady-state dc conditions. In practice though, current will leak off the stack through the voltage-sensing circuitry; this

current leakage will lead to a gradual decrease in the voltage across the stack in accordance with a time constant of 150 ms. As a result, there will be many clock cycles in which there will be no action on the part of the switching circuit because the error between the command and input is in the dead band. Such cycles will be followed by a single clock cycle in which a small correcting step is made. At maximum voltage, these corrections are calculated to occur at about a 2-kHz rate.

## 2.3 DRIVER LOGIC

The control logic consists of four flip-flops, a predictor circuit, and a stack zero-current sensor. The first of the four flip-flops is the rise flip-flop. Its state determines whether the next clock cycle will result in the stack's voltage being increased or decreased. The second flip-flop directly turns on or turns off the driver transistors. The third flip-flop provides the commutating signal for the driver transistors. The fourth flip-flop turns on or off the high-voltage transistors. The rise flip-flop is set at the midpoint of each clock cycle to a state determined by the polarity of the error signal.

The function of the predictor circuit is to turn off the drive flip-flop μ10(b) (Figure 6) once it has been turned on. It is turned on if, at the beginning of the clock period, a difference between the command and actual stack voltage of more than one-half percent full-scale exists. The predictor circuit calculates the interval during which this flip-flop must be on. The correct time interval for any given initial stack voltage, direction of change and magnitude of change is shown by the family of curves in Figure 15. Part of the predictor circuit is concerned with choosing the correct curve from the family. This part is active during the latter half of the previous clock cycle. The stack voltage divided by 150 $V_{SC}$ is scaled linearly with respect to the state of the rise flip-flop μ10(a); the resulting signal $V_{SL}$ is used to generate




$t_c$ is internal transitor on time

$V_s^{PS}$ is stack swing resulting, referred to primary

N = 16, $V_{bb}$ = 112.5, τ = 160 μsec, $V_s^{PO}$ is initial stack voltage referred to primary

Figure 15. Transistor pulse width versus required stack voltage change.

a nonlinear signal $V_{SN}$ by comparing it to the common ramp $V_{RA}$, and using the instant of comparison to sample the nonlinear ramp $V_{XP}$ (Figure 16). This voltage $V_{SN}$ as held by the sample-and-hold amplifier μ5 is delivered ($V_{SN}$) to the integrator circuit (see Figure 16). The second step of the predictor process occurs in real time and is the result of the continually rising ramp $V_{CR}$ produced by the integrator. This rising ramp occurs in response to current flowing through the analog switches actuated by the series of common logic signals, $L_{R0}$, $L_{R1}$, $L_{R2}$, $L_{R3}$ and $L_{R4}$. The effect of closing these switches, first one at a time and then in groups, provides a rising ramp at the integrator output that begins as a very gradual voltage slope and then continues to an ever steeper slope (see Figure 17). This ramp is now compared to a voltage, $V_{CS}^{H}$, based on the difference between the commanded and actual voltage to the load, and when the ramp exceeds that voltage a signal develops that causes the drive flip-flop μ10 to be reset.

When a falling ramp condition exists (i.e., an absolute voltage of more than 300 volts exists on the stack, and the stack is being discharged), the "D" input to the commutating flip-flop μ13A is high. It is set by the action of the clock pulse $L_{CC}$ arriving from the common logic at a point in time safely after the predictor circuit has reset the drive flip-flop. The commutating flip-flop remains set until the high-voltage flip-flop is reset.

The stack current is monitored by a current transformer $T_2$, and this input to the comparator μ4B results in a rising edge or falling edge output at a point just before the stack current returns to zero. There is a bias circuit from the rise flip-flop that causes this crossover point to be slightly above zero in the case of a rising ramp and slightly below zero in the case of a falling ramp (see Figure 7). This signal change is propagated through the action of appropriate steering logic, again from the rise

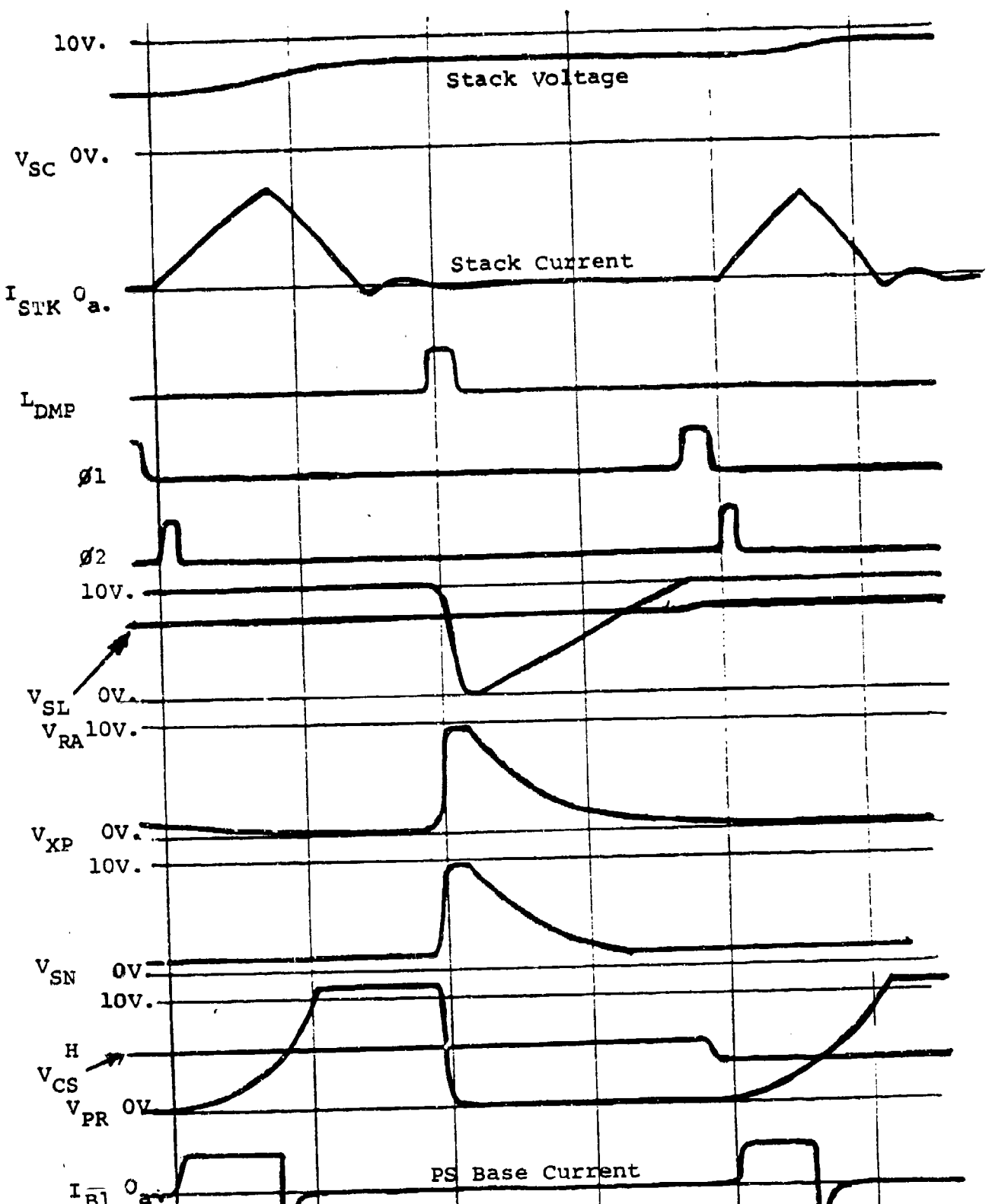
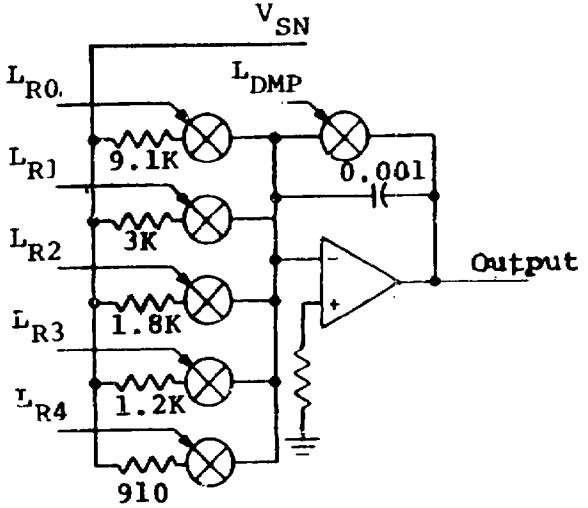
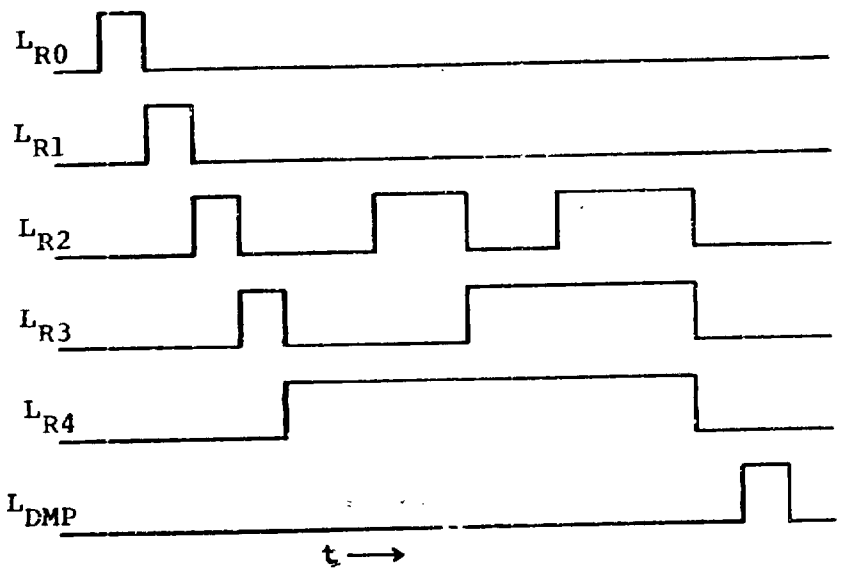


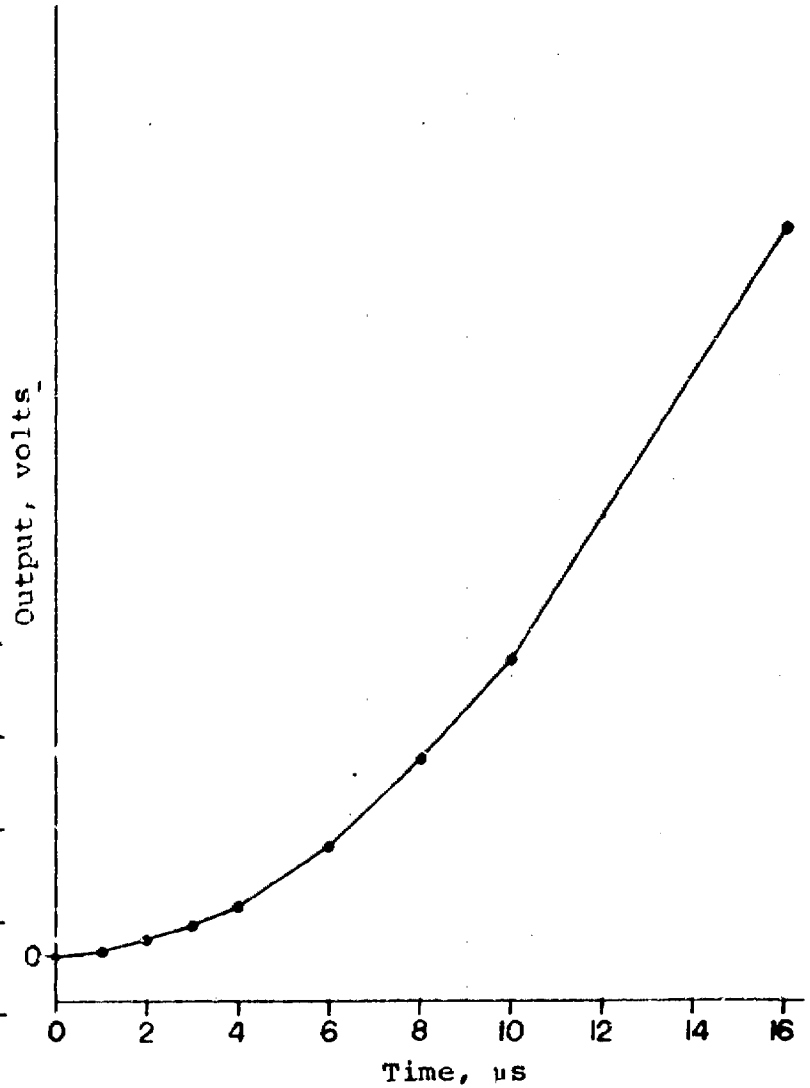

Figure 16, System time line.




a




b




c

Figure 17. Logic integrator.

flip-flop, to turn off the commutating flip-flop and the high-voltage output transistor turn-on flip-flop ($\mu$13B). Backup signals from the common logic will turn off the three flip-flops (the drive, the commutate, and the HVG) at $L_{DMP}$ time if for any reason the normal signals should fail to do so. $\overline{POR}$, containing negative going pulses at $L_{DMP}$ time, is coupled through NAN: $\mu$11B to CLR of $\mu$10B to reset the TRNON flip-flop, and $L_{DMP}$ itself is coupled through NOR $\mu$15B to reset the COMUTX and HV flip-flops. By this means, runaway conditions c[illegible] by saturated inductive components are prevented.

## 2.4 FAULT PROTECTION

A major concern in the design and construction of a multi-channel system is the propagation of failure from one amplifier to others, either by depriving them of power or by causing component failure. In this application, it is very desirable for an amplifier failure to result in its output becoming a short circuit. Since the load in this design is assumed to be capacitive, and only a small voltage change is expected to result during any clock cycle, a change of zero volts as a result of the action of the circuit will not disturb or defeat the proper operation of the circuit. Therefore, the system is inherently resistant to damage by short circuits. Various types of short circuits in the high-voltage section will not cause a catastrophic failure of the multi-channel amplifier system. The worst that could happen is that the load of the affected channel would be discharged to zero volts. Failures in the logic or the base driver circuits for the driver transistors could result in either no drive or a continuous drive signal to one or both drive transistors. In the latter case, the fuse to that channel would blow to allow the 112-V power supply to remain active to the other channels. A driver transistor that shorts collector-to-base will try to pass high voltage to its base circuit; this condition will cause the SCR ($Q_{11}$ or $Q_{12}$) to turn on, shorting the base to ground and so the 112-V supply until the fuse blows.

## 2.5 COMMON LOGIC

The common logic is designed to minimize the parts count of the channel amplifier logic by providing a series of digital and analog signals to the channel amplifiers via a bus system. It implements all functions that occur uniformly in every channel during every clock cycle.

In Figure 16, several of the signals from the common logic are shown as they arrive in the channel logic via the bus lines. The digital signal $\phi 1$ causes the sampling of the control-error signal $V_{CE}$ for the cycle about to begin. $\phi 2$ turns on the PS and HVG transistors through their control flip-flops if an error signal exceeding the deadband is present. $L_{DMP}$ (Figures 16 and 17) dumps the predictor ramp integrator, and $L_{RO}$, $L_{R1}$, $L_{R2}$, $L_{R3}$ and $L_{R4}$, (Figure 17) acting through analog switches, generate the predicting ramp. The analog signals $V_{RA}$ and $V_{XP}$ act as described above in selecting the correct predicting curve. Not shown on Figure 16 are digital signals GUARD and $L_{CC}$, which prevent race conditions and turn on the commutating flip-flop when appropriate; in addition, Figure 16 does not illustrate POR, the power-on-reset signal, which also contains a back-up pulse to reset the flip-flops if the normal signals should fail to do so.

In the common logic is a 1 MHz crystal oscillator that drives a modular 40 counter which overflows at a 25 kHz rate. Various counts of the counter are decoded and combined in groups to generate the digital signals described above. An integrator, dumped and gated by appropriately decoded digital signals, produces $V_{RA}$. A capacitor is charged and discharged through a resistor by appropriately gated signals to produce $V_{XP}$ through an analog follower.

Power-on-reset circuitry is provided and produces POR. The mod 40 counter is initialized by the power-on reset circuitry at $L_{DMP}$ time (cycle 20). The digital outputs are buffered by bus drivers which have the capability of fanning out to 61 loads.

## 2.6 SIGNAL INPUT

The input impedance is 100 kΩ as can be seen in Figure 5. Under saturation conditions (up to ± 40 V on input) the impedance drops to 2 kΩ. The input capacitance can be considered to be the value of a maximum of three feet of RG-174 shielded cable, i.e., 100 pf or less. There are no circuit elements introducing input inductance, and, since the ground return of the shielded cable is connected directly to the circuit trace that grounds the load resistor input or amp, that inductance should be only a few nanohenries. On Figure 5 will be noted two back-to-back 1N5535s (zener diodes). These have a zener voltage of 15 V and, downstream from the 2-kΩ resistor, serve to protect the input op amp against any high voltages that may enter on the input lines.

The gain adjustment is made by adjusting the trimpot $R_5$, loading the output of the precision rectifier, and referencing it to ground. The offset adjustment is made by adjusting the trimpot connected from -15 V to +15 V, which has its wiper connected through a resistor to the summing junction (see Appendix G).

# SECTION 3

# TESTING AND MODIFICATION

This section presents the results of: (1) component tests in a breadboard simulating worst-case circuit conditions; and (2) debugging of the prototype 2-channel amplifier circuit. Each set of tests resulted in design modifications. The principal modifications were made as a result of the breadboard tests. There were many changes required during debugging, but all were relatively minor.

## 3.1 BREADBOARD TESTING

In the initial phase of the program, a breadboard circuit was fabricated to explore certain worst-case conditions arising from the juxtaposition of circuit components. This work resolved many feasibility questions and also pointed out a number of design and construction problems that were initially unsuspected, but were subsequently analyzed and solved. A summary of this breadboard effort is presented below, and the circuit schematic is shown in Figure 18.

SCRs were originally planned for the high-voltage switches, because only a pulse of gate current is required to turn on an SCR, and they can be easily referred to a floating reference that can float to high voltage (up to 2 kV was anticipated). But component testing was required to ensure feasibility of SCRs in an application requiring fast commutation, high dV/dt rates,

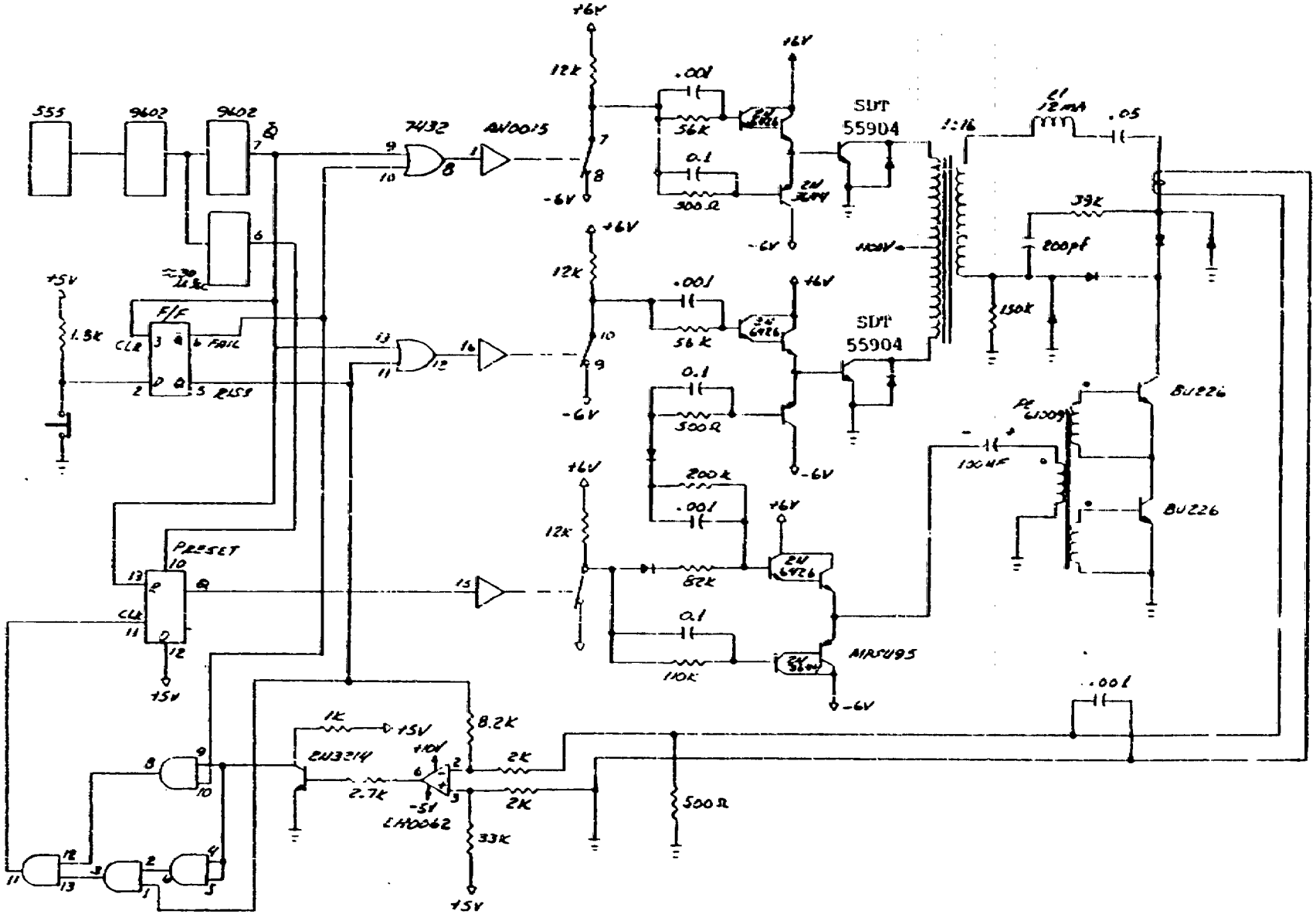



Figure 18. Breadboard schematic.

high initial turn-on rates (high dI/dt), high breakdown voltage, low leakage, low gate-trigger current requirements, and suitable package size. Testing was also required to select the optimum SCR among several candidates.

Originally, plans had been made to perform a series of tests on certain components, in particular the SCRs. In these component tests, each electrical characteristic (viz., breakdown voltage and leakage, commutation, dV/dt, dI/dt, and gate-trigger current) was measured in turn. The SCR tests yielded confusing results, for an SCR acceptable in one characteristic was generally not so acceptable in others. Evidence mounted that while an SCR might attain a certain level in a given characteristic by itself, it might not do well when the characteristic was tested in combination with others.

In an attempt to resolve these doubts, the components evaluation task was expanded to include a rough breadboard of the power-switching stage of one actuator channel, a dummy load, and enough logic to test certain worst-case conditions. At this time, results obtained from the computer modeling program, when applied to the data obtained from the separate SCR tests, predicted that SCRs would not be feasible as a high-voltage switch. Soon afterwards, results from the newly constructed breadboard confirmed this prediction.

A design modification was made to use high-voltage NPN transistors in a full-wave bridge configuration for the high-voltage switch. The computer program was modified accordingly, and indications were that the design was feasible, but high transient voltages (up to 3.4 kV) would be present in certain conditions. Several candidate high-voltage transistors were ordered for a

series of individual characteristics tests (viz., high-voltage breakdown and leakage, saturation beta, and turn-off time) and for test evaluation in the breadboard. The test data did not highlight an obvious choice; there were several trade-offs to consider.

Results from the power switching (PS) transistor tests, after initial screening for candidates, are shown in Table 2. These transistors were tested for feasibility to collect data on expected circuit power losses and to optimize the base driver circuit. Specifically they were tested for: (1) saturation voltage (under pulse conditions) with 15 A collector current; (2) saturation beta (namely collector current-base current to hold device in saturation) with 15 A collector current; and (3) turn-off time in a resistive circuit with 15 A current before turn-off and 220 V after turn-off. High-temperature (160$^{o}$F) and low-temperature (-70$^{o}$F) tests as well as room-temperature tests were made.

Results obtained from the breadboard were at variance with those obtained from the computer program in certain respects. Large amounts of voltage and current ringing were found to be due to interwinding capacitance of the transformer $T_1$ (see Figure 10). It was found that if the secondary was wound on a thrice-segmented bobbin so as to reduce this capacitance, the ringing could be minimized. The inductor $L_1$ was also rewound on a thrice-segmented toroid; this helped to minimize the ringing. High common-mode voltages appearing in all high-voltage components, including the transistors, just after turn-off were found to be due to primary-to-secondary capacitance in the transformer (see Figure 11); another alternative method of building the transformer was found to reduce the amount of energy lost as a result. Subsequently, it was found that the capacitance of the transistors themselves also cause this effect; it is controlled by a combination of closely controlling the transformer magnetizing inductance and a zener diode clipping network (see Figure 12).

TABLE 2

TRANSISTOR TESTS

| A. Power Switching (PS) Transistor Candidates | TRW SVT-450 | SOLITRON SDT 55407 | DELCO DTS 4075 |
|---|---|---|---|
| Case Size | TO-3 | TO-63 | TO-3 |
| Saturation Beta | 5 (@ 9 A) | 30 (@ 15 A) | 50-60 (@ 15 A) |
| Saturation Beta at High Temperature (180°F) | Similar | Similar | 30-40 |
| Turn-Off Time | 0.05 μs (at 3 A) | 0.15 μs (at 15 A) | 1 μs |
| Turn-Off Time at High Temperature | 0.1 μs | Similar | 5-15 μs |

| B. High-Voltage Gate (HVG) Transistor Candidates | SYLVANIA ECG 238 | TELEFUNKEN BU226 | MOTOROLA BU108 | MALLORY PTC130 |
|---|---|---|---|---|
| Breakdown (Room Temperature) | 1900-2100 V | 2300-2500 V | 1600-2100 V | 2100-2300 V |
| Breakdown (High Temperature-180°F) | Similar | Similar | Similar | Similar |
| Delay on Turn-off | 2.1 μs | 1.5 μs | 1.0 μs | 1.6 μs |

As a result of the breadboard tests, components could be selected for the final design with a much greater level of confidence. In the case of the PS transistors, the Solitron 55407s seemed initially to be the obvious choice. They were very fast, had high beta even at maximum current, and their characteristics did not drastically deteriorate with temperature. However, they were extremely sensitive to instantaneous overvoltages. Later in the program it also became evident that they had a low tolerance to reverse-bias secondary breakdown. In addition they were quite expensive and difficult to obtain. These considerations led to a closer look at the Delco DTS 4075; it was found that with proper component values for the base drive circuit it could perform with less turn-off time than originally found in testing; turn-off times of 0.6 μs were obtained typically. Subsequent to the use of the Delco, a fourth candidate, the TRW SVT6002, was evaluated and found to be similar to the Delco, but with somewhat improved beta and high-temperature characteristics. A decision was made to select the TRW transistor.

In the case of the HVG transistors the initial choice was the Motorola BU108, based on turn-off time and resistance to secondary breakdown in the application. Subsequently, the BU208 was evaluated and was found to be similar to the BU108, but with higher beta. The higher beta characteristic permitted the base drive circuit to be operated at lower current levels and, therefore, lower dissipation.

## 3.2 FABRICATION AND DEVELOPMENT TESTING

After completion of the breadboard testing and final component selection, the two-channel prototype was fabricated and tested to determine operating characteristics. As in any prototype construction, some redesign was found necessary during the developmental testing phase. To minimize the total effort expended in this task, debugging tests were conducted first on a single channel; modifications made to the first channel were generally incorporated into the second only after debugging was complete and all circuit modifications had been identified. Specific problem areas encountered during this test program are discussed in the ensuing sections.

3.2.1 Channel Step-Up Transformer. Particular problems were encountered with the transformer ($T_1$) design during circuit debugging. The transformer (see Figure 8) was modified several times. A larger size transformer was required to prevent saturation with a high-voltage dc or when responding to a step of nearly the full voltage swing (-1500 to +1500 V). For the size selected, saturation can be prevented only by appropriately reducing and controlling the magnetizing inductance with an air gap; this change causes some compromise with circulating currents and leakage inductance and losses. More important, the losses at full slew-rate amplitude are much higher, mostly because with more volume of ferrite, there are more ferrite or "iron" losses. The temperature rise in the transformer would surely cause failure if a 400 Hz, full-amplitude sine wave were sustained indefinitely. However, if the transformer is properly mounted and heat-greased to the heat sink with water flowing through, it should be able to survive the one-minute-on, one-minute-off test given in the statement of work.

The turns ratio was also changed because the effective turns ratio was found to be different from the actual due to coupling of circulating currents from ringing and internal capacitances. The actual turns ratio is 19 to 1 to achieve a desired effective turns ratio of 17 to 1. It is suspected that to some extent the effective turns ratio also changes with the air gap. Some optimization work involving the transformer remains to be done.

3.2.2 Transistors. Another problem area discovered during debugging was the high-voltage gate (HVG) transistors. These have an internal nonlinear capacitance, which is augmented somewhat by the base coupling transformer $T_3$. This transistor forms a resonant tank circuit with the $T_1$ transformer magnetizing inductance, acting through the diode quad (Figure 11), and is excited by the load voltage when the HVGs turn off. Very high voltage would ring up across the HVGs, particularly when the load voltage was high. Although $T_3$ was redesigned to reduce its contribution to the capacitance, it was necessary to provide a high-voltage zener to shunt some of the energy of the tank from pure voltage across the HVGs. After unsuccessful experimentation with power diodes acting in the avalanche mode, a string of zeners with balancing resistors was added to each HVG transistor (Figure 12). Such strings can be made in quantity as hybrid modules, as is done currently with high-voltage diodes. The zeners conduct when the voltage across each string exceeds 1200 V.

The base drive circuit for the HVG was also modified to provide more even distribution of base current to the two devices and to effect faster turn-off of the devices.

The power switching (PS) transistors were changed from the Solitron SDT 55407 to the TRW SVT6002 type. The latter were considered in the early part of the program as a second choice to the

Solitrons, but they were ultimately selected for their superior resistance to voltage and current transients, even though they dissipate more power. They are also more inexpensive and readily available than the Solitrons.

Some under-design of the driver circuit of the PS transistor was found and corrected. The PNP and the NPN driver were made both darlington. It was also discovered that the TRW transistor, as well as the second source choice, the Delco DTS-4053, can burn out to a collector-to-base short, base-to-emitter open condition, resulting in high voltage on the base and on the two darlington drivers. The PNP driver would then conduct large amounts of current into the -7 V supply, saturating it and reversing the voltage so as to cause a train of failures in PNP drivers of other channels. To prevent this, an SCR was added to the base circuit of each PS transistor (Figure 8). This SCR turns on only in a catastrophic failure mode involving excessive positive base voltage to shunt current to ground and thus not involve the -7 V supply.

3.2.3 Common Logic. There were a number of timing changes made to the common logic. The correct time relationships now existing are shown in Figures 16 and 17. The major reasons for the changes were:

1. A new signal $L_{CC}$ was created to turn on the commutating (COMUTX) flip-flop, so that the appropriate PS transistor, always opposite the one providing the drive, would turn on only after the drive transistor was safely off;

2. A new GUARD signal was created to turn on the TRNON and HVG flip-flops without race conditions;

3. A pulse was added to the POR signal to "back up" the normal signals turning off the TRNON, COMUTX and HVG flip-flops should they for any reason fail;

4. Signals to the analog switches were arranged to be at least 2 μs wide, to lessen the system's dependence on the variability of switching time of these analog switches;

5. The $\phi 1$ and $\phi 2$ signals were separated by 4 μs to allow μ7, providing $V_{CS}^{H}$, more time to capture an accurate signal.

3.2.4 Current Sensor. The design of the current sensor was refined with appropriate channel logic to implement its signals. A bias circuit arrangement, deriving from a signal from the RISE flip-flop, was added to effect the current turnover point at near zero amps, but away from zero so as to avoid noise amplification right at zero amps, and offset in the direction that current is expected to flow. The ground reference point for the stack current loop was also changed to prevent charging current to the HVG capacitance from passing through the current sensor. This change resulted in the current transformer $T_2$ between the low side of the load and ground; however, no more than a volt or so would ever be generated across it. It is important, however, to avoid external grounds on the low side of the load that would provide a bypass current path.

## 3.3 CONCLUSION

During the course of the debugging tests, some fifty modifications were made to the design of the actuator amplifier channels and the common logic. Most of the changes are very minor, and some of them cancelled the effect of earlier changes. As in any first-of-a-kind engineering effort there was over-design in many areas, but this project has such severe size, weight, and power-loss constraints that marginality was often necessary, and a situation of both over-design in some areas and under-design in others resulted. These circumstances complicated the debugging effort. It was further complicated by the presence of three types of circuitry--digital, analog, and high-voltage--each with its own characteristic problems plus those arising from the interactions of the circuit types.

The debugging effort was also complicated by dealing with a scale prototype, that is, one physically laid out as if it were part of the finished 61-channel system with its severe size constraints; thus the parts were compressed to an unusual degree. Nevertheless, the earlier breadboard effort expedited the debugging effort by identifying and solving many problems before the prototype was constructed.

# SECTION 4

# PERFORMANCE

## 4.1 INTRODUCTION

Following completion of debugging and circuit modification, performance evaluation tests were conducted on the two-channel system. The objectives of these tests were to determine the impulse-response function for each channel separately and for the two together. Power consumption, linearity, slew rate, gain, and cross-coupling, were measured for a range of input voltages, waveforms, and frequencies. Drift was measured with a constant input of 6.5 V. Specific test levels are listed in Table 3 for the single channel performance tests and in Table 4 for the dual channel tests.

Sine wave tests, at 5 percent full amplitude, were performed over a range of frequencies from 1 Hz to 1 kHz; a sufficient number of points was taken to permit a Bode plot to be made. Sine wave tests were also conducted at 100 percent amplitude over a range of frequencies from 1 Hz to 1 kHz; Bode plots were also made of these.

Square wave tests were conducted at 400 Hz with 5 percent, 50 percent, and 100 percent full amplitude. These showed the slew rate, the settling time, and the nature of the switching noise.

TABLE 3

SINGLE CHANNEL PERFORMANCE TESTS

| Type of Test | Characteristic Measured | Test Levels |
|---|---|---|
| DC | Power consumption<br>Switching noise | 0 V, 500 V, 1000 V, 1500 V output |
| Ramp<br>(triangle wave) | Linearity | 1 Hz: 0.5 V, 5 V, 9 V input<br>100 Hz: 0.5 V, 5 V, 9 V input<br>625 Hz: 0.5 V, 5 V, 8 V input |
| Step<br>(square wave) | Settling time<br>Risetime overshoot<br>(slew rate) | 1 Hz: 0.5 V (peak), 5 V, 8 V, 1.5 V (peak), 0-3 V square<br>100 Hz: 0.5 V, 5 V, 8 V |
| Sine Wave | Power consumption<br>Frequency response | 0.5 V input: 1 Hz, 2 Hz, 5 Hz, 10 Hz, 20 Hz, 50 Hz, 100 Hz, 500 Hz, 1000 Hz<br>9 V input: 1 Hz, 2 Hz, 5 Hz, 10 Hz, 20 Hz, 50 Hz, 100 Hz, 500 Hz, 1000 Hz |

TABLE 4

DUAL CHANNEL PERFORMANCE TESTS

| Type of Test | Characteristic Measured | Channel 1 | Channel 2 |
|---|---|---|---|
| DC | Cross Coupling | +5 V in dc<br>0 V in dc<br>+5 V in dc | 0 V in dc<br>-5 V in dc<br>-5 V in dc |
| DC and Sine Wave | Cross Coupling | +5 V in dc<br>-5 V in dc | ±5 V sine wave at 100 Hz<br>±5 V sine wave at 100 Hz |
| Triangle Wave and Sine Wave | Cross Coupling | 5 V peak triangle at 1 Hz | 5 V peak sine at 100 Hz |
| Sine Wave | Cross Coupling | 5 V sine wave at 80 Hz | 5 V sine wave at 250 Hz |
| DC | Drift | 1000 V output | 1000 V output |

Triangle wave tests were performed at 1 Hz, 100 Hz, and 625 Hz; these were analyzed to determine linearity. The dummy loads provided for the tests were capacitors, each having a capacitance of approximately 0.05 μf, consisting of a combination of mica and disk ceramic capacitors such that the D-E curve closely approximates the D-E curve of PZT-8 stack material.

A function generator produced dc voltages and sine, square, and triangle waves of various frequencies. The function generator output and the amplifier output were monitored and recorded on tape with the Norland Model NI2001A programmable calculating oscilloscope (PCO). The raw data tapes generated have been provided to the AFWL. To determine power losses, ammeters and voltmeters were provided on the 112 V, +7 V, and -7 V supplies. Nearly all the power dissipated in the circuit is provided by these three supplies; the others provide merely a small amount of logic power.

The setup of the tests is illustrated in Figure 4, which shows the interconnection of the PC boards, the common logic breadboard, and the laboratory bench supplies. The Norland PCO is connected to inputs and across loads as appropriate. A complete list of the equipment used in these tests is given in Appendix J.

During the test program, intermittent problems were encountered in the channel 4 input or the Norland. It had a variable offset that drifted erratically with time, in the manner of semiconductor "pink noise," with the greatest amplitude in the range of 0.1 Hz to 5 Hz. That is, if the input coupling were set at GND, the voltage read for that channel, if displayed on the screen, would vary ±10 percent of full scale in a random pink noise manner. If a real signal were input, the pink noise would be present on top of this.

This problem arose from an idiosyncrasy of the Norland. An offset would develop in all the elements of an array in the process of stopping the moving array with either the TRIGGERED HOLD or the PERIODIC HOLD feature. It can be shown that when the instrument is in RELEASE, the correct dc voltage will be displayed on the screen (and read through the cursors) "on the fly," but the reading will change by some offset error of up to ±10 percent when the array is stopped. This problem has occurred intermittently on all the Norland inputs. In the case of channel 4 (i.e., the "B" channel of the right-hand plug-in), this problem has gradually worsened until it has become as described above.

During performance tests there were certain component failures. In conducting dc tests on channel 8, it was noted that at a little above 1350 V, a catastrophic increase in current of the 112-V supply set in, suggestive of some mode of saturation. This was not noted on channel 7.

In the process of running the step tests, some burnouts occurred in channel 8. These were encountered during the +10 V to -10 V (input voltage) steps. In each case, $Q_7$, its associated SCR, and the associated PNP darlington driver $Q_2$ would burn out; these components were replaced. In one case an abnormally slow-acting $Q_7$ was encountered; it resulted in very low slew-rate response for steps from zero to maximum negative. In another case the HVGs, $Q_9$ and $Q_{10}$ were found damaged and were replaced. One diode in the diode bridge, $D_{15}$, was also damaged; all the diodes were replaced. It was found necessary to restrict the maximum voltage during the step tests to 1200 V to prevent further burnouts.

Channel 7 also experienced a burnout during the step tests, involving $Q_8$ and its associated SCR. A diode $Q_5$ was also found

bad, and it was replaced. During the last stages of the cross-coupling tests, the wire in the cabling, carrying the voltage feedback between the main amplifier board and the logic board, broke and caused channel 7 to fail. By the time the cause of failure was found and corrected, $L_9$, $L_{10}$, and the four bridge diodes had been replaced on the (incorrect) assumption that they were the cause of the problem. These failures (with the exception of the broken wire) are believed to be due to transformer saturation that is still occurring under the same conditions (maximum voltage dc or full-amplitude slews).

Performance characteristics of the two-channel prototype observed during this test program are described in the following section.

## 4.2 POWER CONSUMPTION

Power consumption was one of the objectives of the dc tests and also of the ac sine wave tests. Power dissipation is determined by measuring the voltage and current output by the three supplies to the power stage: the +112 V, the +7 V, and -7 V. Since in the tests these voltages are provided by regulated supplies, the voltages were set before the first test of each day and occasionally monitored to verify that the supplies were working and regulating. The currents were monitored for each test. The power dissipated is:

$$W_{(watts)} = V_{bb}I_{bb} + V_{+7}I_{+7} + V_{-7}I_{-7}$$

where the subscripts bb, +7, and -7 refer to the 112 V, +7 V and -7 V supplies respectively.

For the sine wave tests, input voltage is taken as the peak-to-zero voltage, and output is taken as the average of the (absolute) peak of at least ten negative half cycles and at least

ten positive half cycles. Power consumed is plotted against dc voltage in Figure 19a and against frequency for the ac tests in Figure 19b. As can be seen, the power losses increase drastically as the maximum slew-rate condition is approached. Most of the losses occur in the transformer $T_1$ and the PS transistors $Q_7$ and $Q_8$, with some losses also occurring in $L_1$, $R_7$, and the zener strings.

## 4.3 LINEARITY

A program was prepared for the Norland PCO to reduce the data gathered for each test to determine the slope, standard voltage deviation, and linearity of single-ramp slopes. The listing for this program appears in Appendix I. To obtain these values, the P cursor is positioned at a point near the beginning of a slope, but within it, and the Q cursor is positioned near the end of the slope, but within it. Voltage and time at P, and Q-P are stored. The slope m is

$$m = \frac{\Delta V}{\Delta t}$$

The standard deviation voltage is the rms of the voltage deviation of each point of the array from a straight line drawn from the stored cursor points, e.g.,

$$V_d = \sqrt{\frac{1}{N} \sum V_{di}^2}$$

where N is the number of points in the array and

$$V_{di} = V_i - \frac{t_i - t_p}{\Delta t} \Delta V - V_p$$

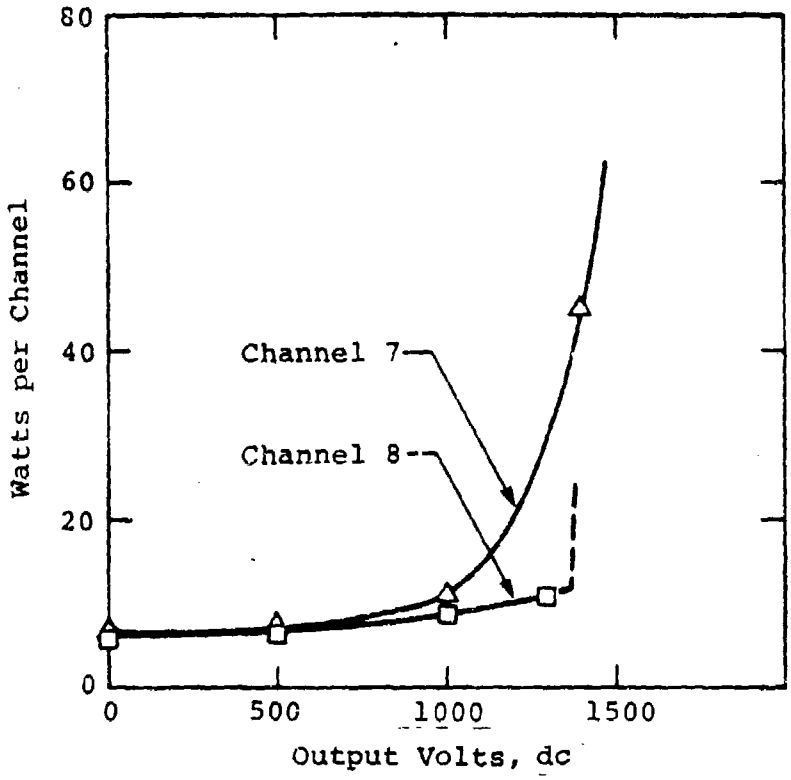



Figure 19a. Power consumption versus dc voltage output.

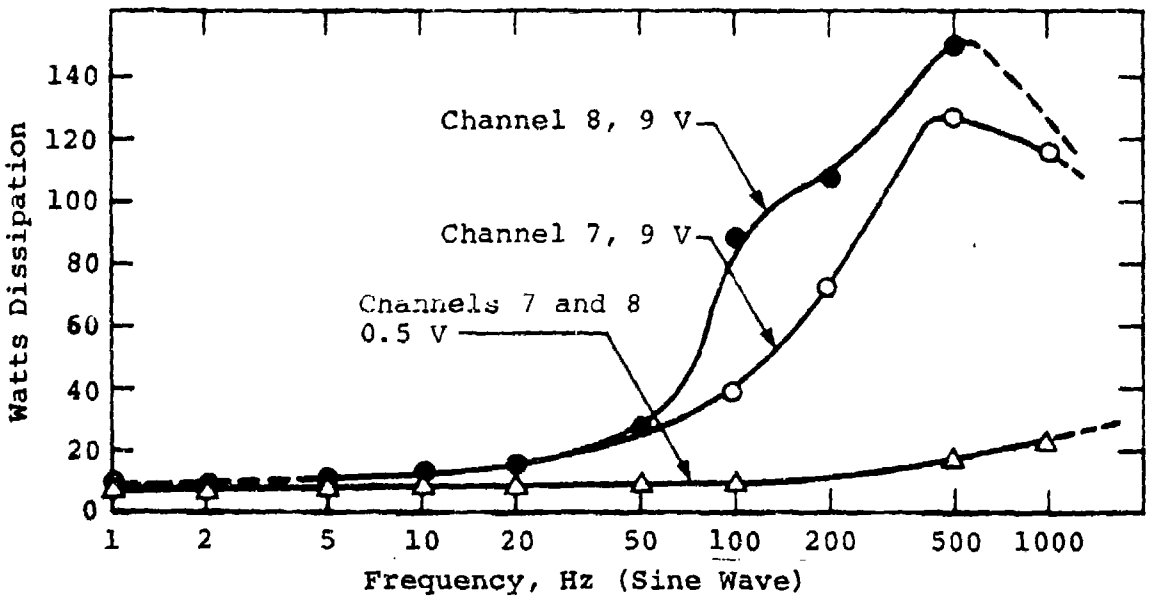



Figure 19b. Power consumption versus ac frequency.

where $V_i$ is the voltage at the ith point, to the ith time, $t_p$ and $V_p$ the stored cursor P time and voltage, and $\Delta t$ and $\Delta V$ the stored Q-P values.

The linearity $\sigma$ is

$$\sigma = \frac{V_d}{\Delta V}$$

where $\Delta V$ is either the stored cursor or full scale, as noted.

The program runs properly, but is time consuming; because of time limitations, not all the data have been reduced. From the data that have been reduced, linearity is plotted against amplitude (Figure 20). The data so far reduced indicate that linearity is well within tne 1 percent specification, except where the output signal is slew-rate limited.

A typical output waveform is shown in Figure 21. This figure shows the performance of the amplifier when slew-rate limitations do not take place. When they do, the linearity suffers, as the slew rate is typically not uniform.

## 4.4 FREQUENCY RESPONSE

For sine wave tests, a program in the Norland reduces the stored data and calculates gain. The 112-V current is measured on a Simpson meter. The +7 V and -7 V current is monitored by meters on power supplies. The voltage of any of the supplies can be monitored by a DVM.

The gain G is

$$G = \frac{V^{av}_{pp\text{-}out}}{V_{pp\text{-}in}}$$

where $V^{av}_{pp\text{-}out} = V^{av}_{max\text{-}out} - V^{av}_{min\text{-}out}$

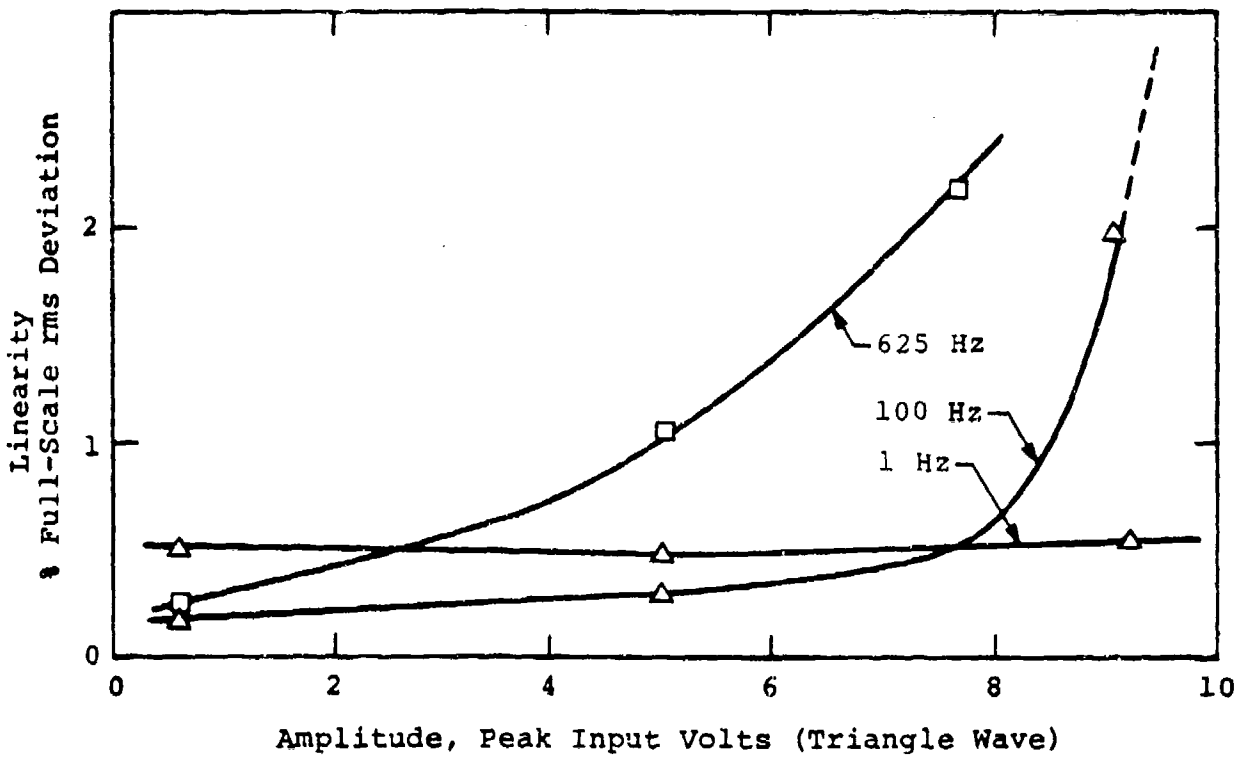
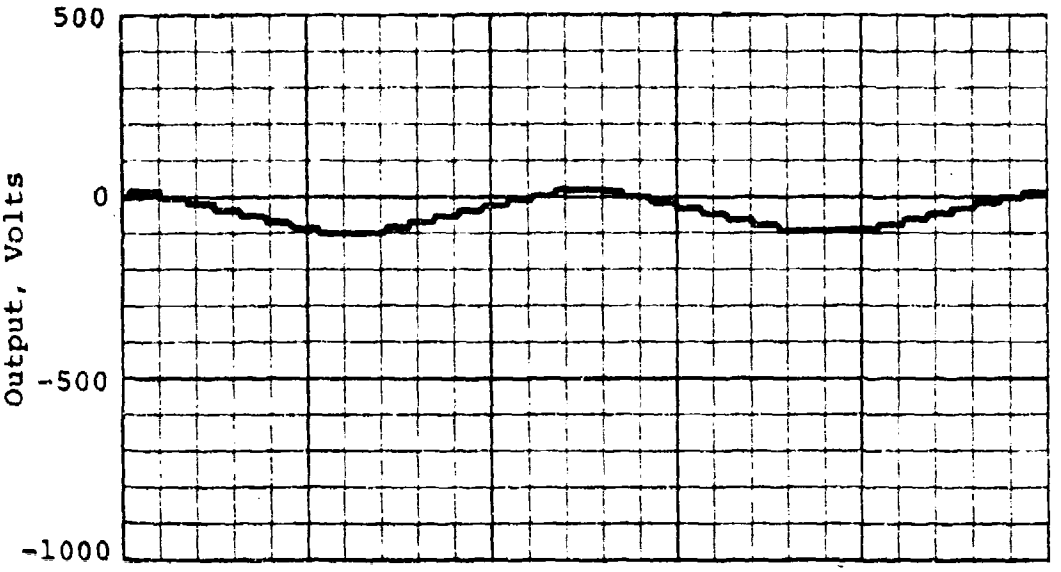
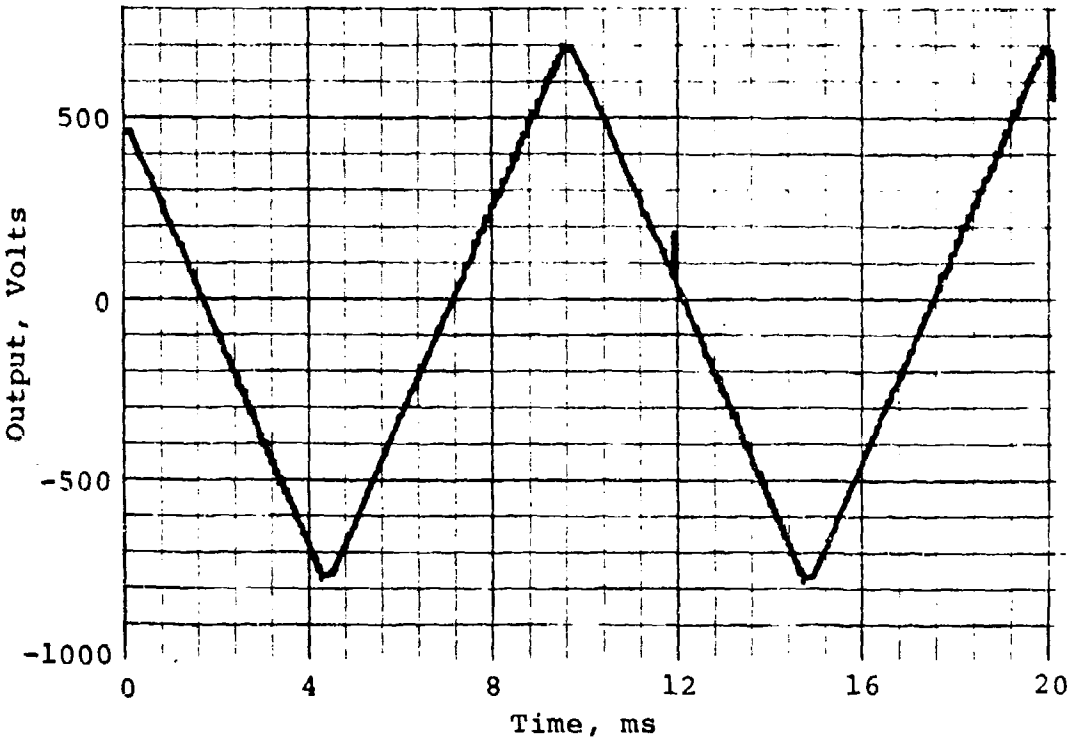



Figure 20. Linearity versus amplitude (Channel 7, triangle waves).




a. 100 Hz, 0.5V peak.




b. 100 Hz, 5V peak.

Figure 21. Typical triangle wave response.

The averages for the maxima and minima are taken over ten consecutive cycles.

Frequency response is plotted from the gain calculated from the data of the sine wave tests. The frequency response itself, for large and small signals, is shown in Figure 22.

Small-signal frequency response is determined from a run of 5 percent full amplitude sine waves (0.5-V peak in) at various frequencies from 1 Hz through 1 kHz. The small-signal response has been observed as high as 8 kHz, even though the test plan calls it out only to 1 kHz. There is evidence that the 3 db point is at least as high as 4 kHz, though the switching noise that exists at these frequencies makes measurement difficult without a special reduction program.

Large-signal frequency response is determined from a run of full amplitude sine waves (10-V peak in) at various frequencies from 1 Hz through 1 kHz. The large-signal response is observed out to the slew-rate limitations (i.e., 400 Hz) except for the particular slew rate problems detailed below.

## 4.5 SLEW RATE

The square wave tests show the slew rate, settling time, and overshoot, if any, for various step sizes. Although the tests were repeated for two frequencies (1 Hz and 100 Hz), the results are essentially the same for both. For each test run, the risetime (10 to 90 percent) is determined with the automatic facility to so do on the Norland; the settling time is then determined by observation. The overshoot, if any, is also determined by observation. Settling time and overshoot are defined in Figure 23.

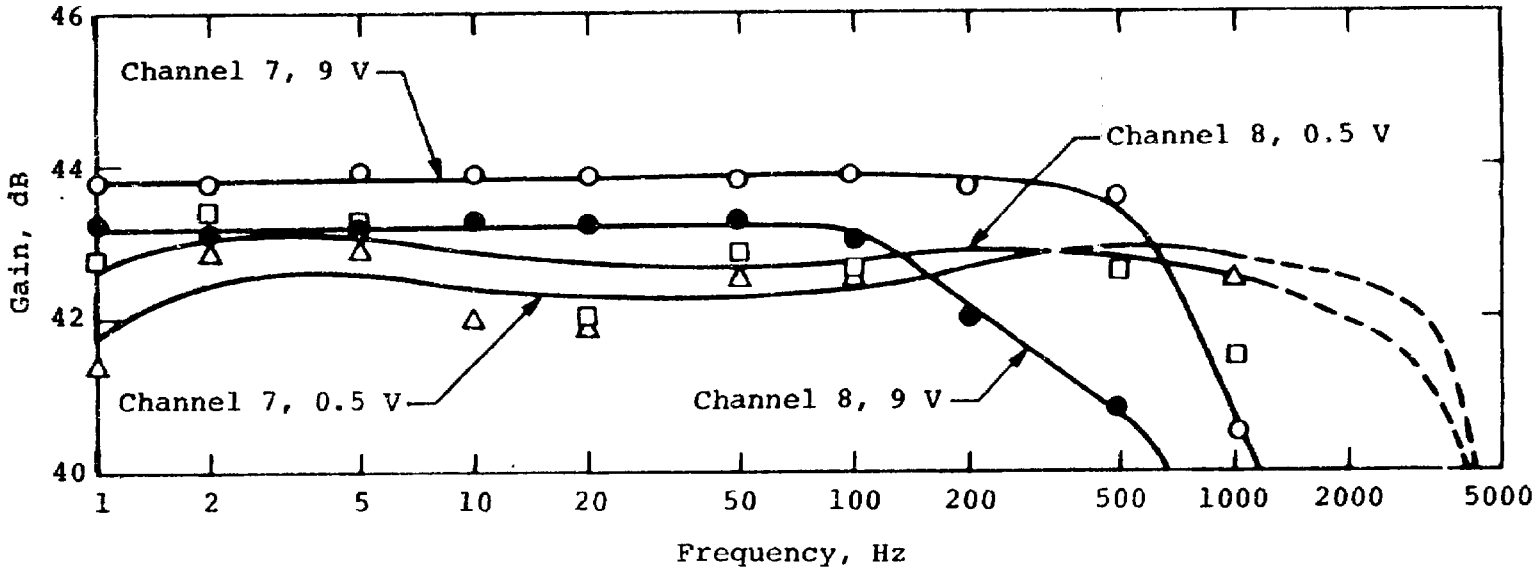



Figure 22. Frequency response to sine wave signals.

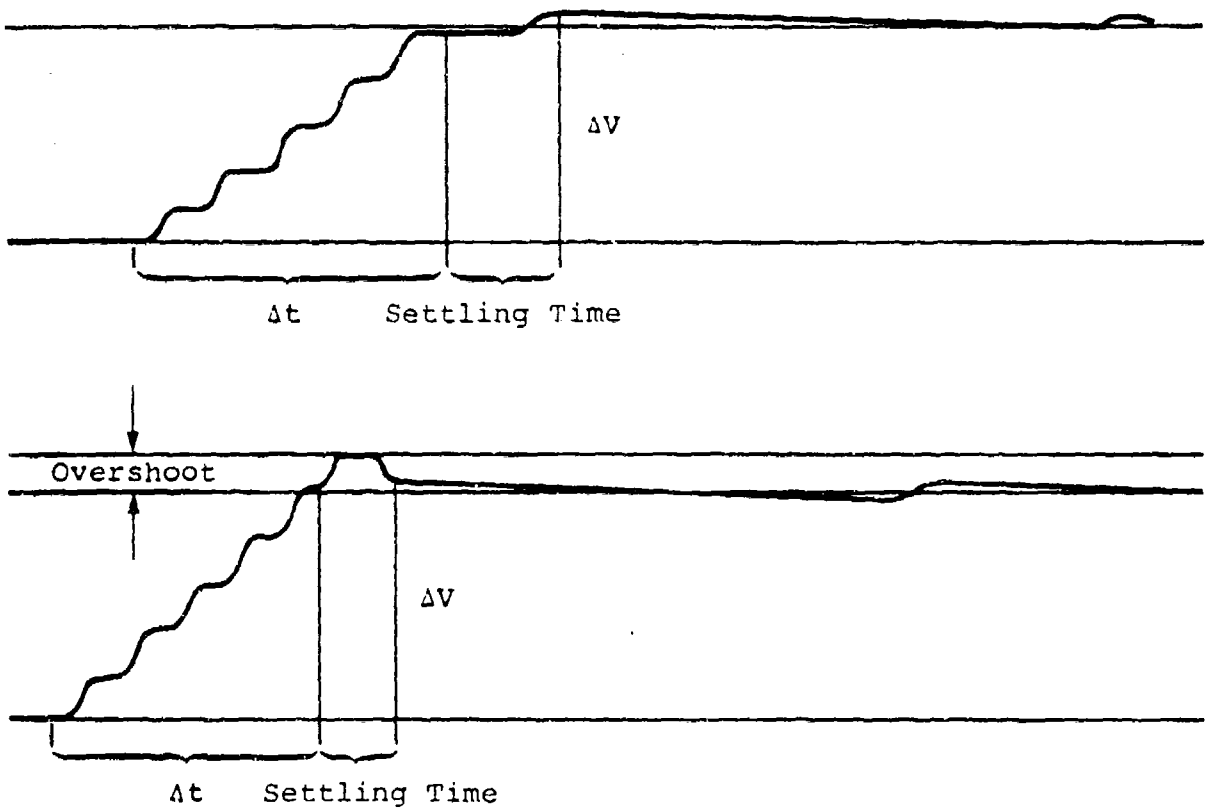



Figure 23. Typical response to step function (square wave) input.

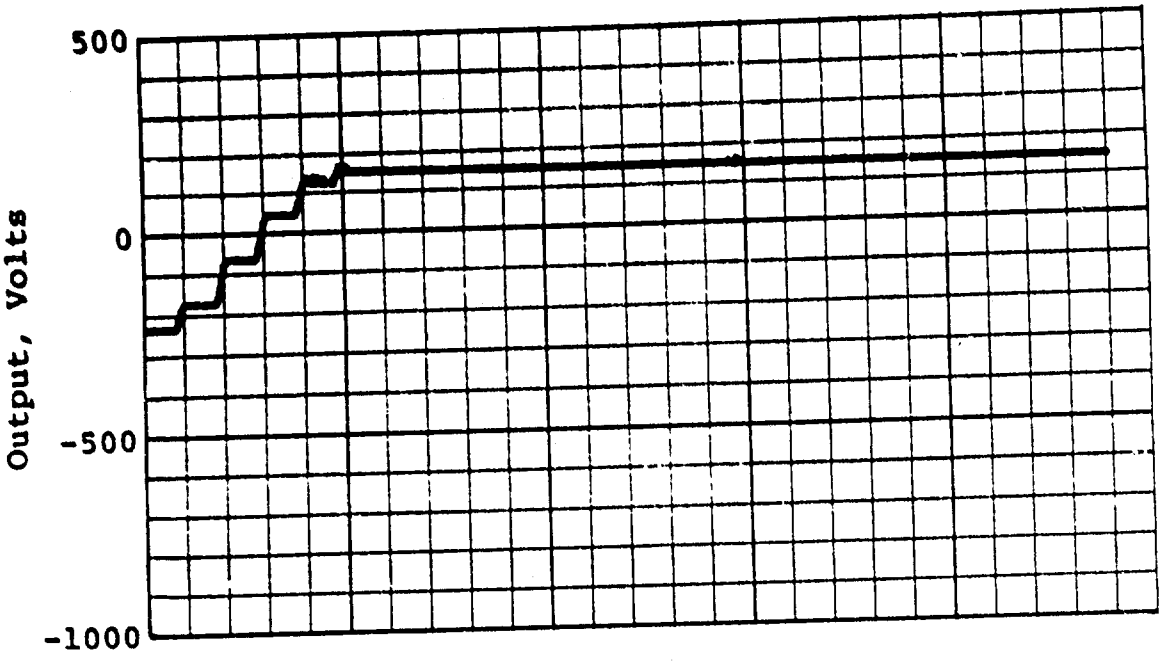
Figure 24 shows typical slew-rate responses to a step input (e.g., the rising edge of a square wave). The figure was made by a X-Y recorder plotting from tapes and is scaled so that the left edge is coincident with the rising edge of the input signal producing the step.

Overshoot is present on many of the square-wave responses. It arises due to deliberate narrow banding in the design of the analog op amps, to reject ringing noise pickup in the analog logic circuitry and to avoid parasitic oscillations in this circuitry. As can be seen in Figure 24, overshoot does not unduly extend the settling time. It would cause a slight increase in switching noise, if it were calculated on an rms basis for these signals.

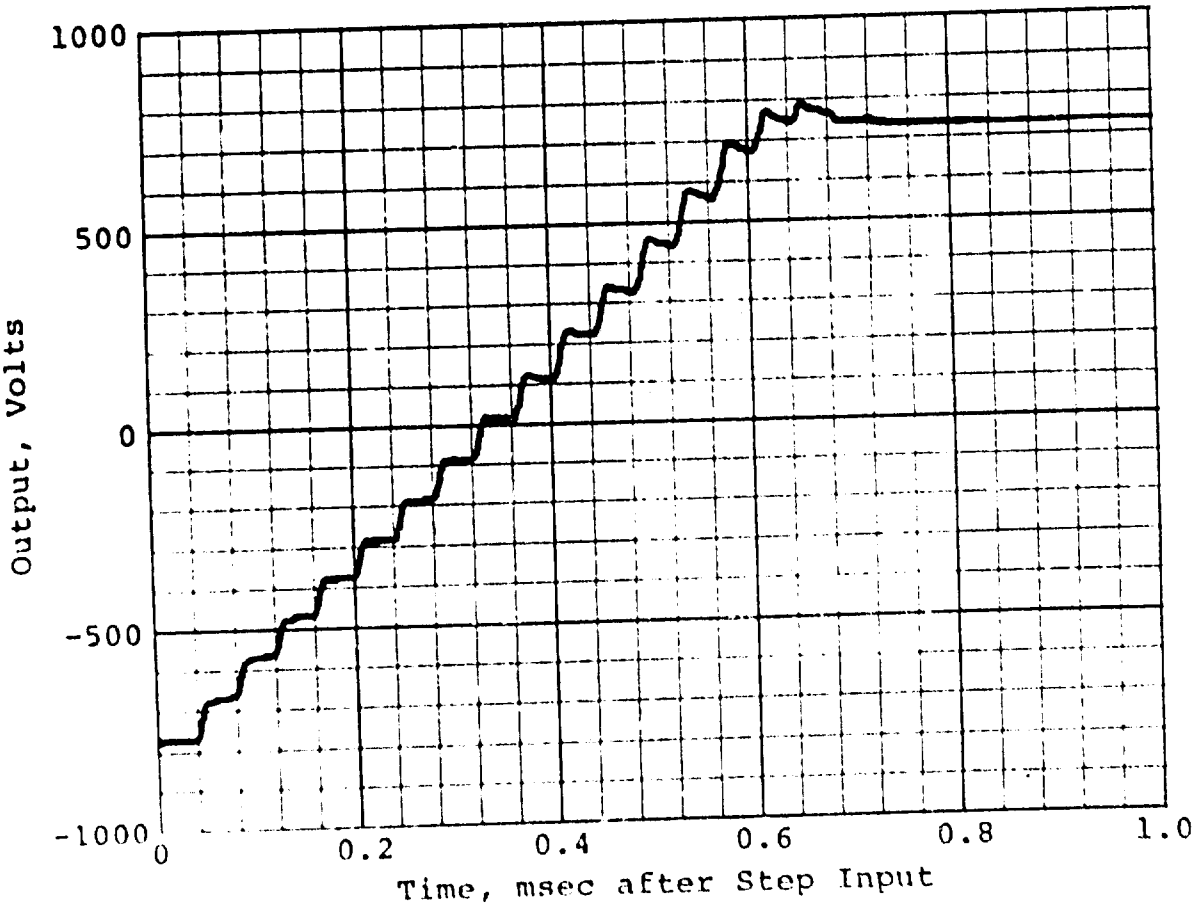
At present the slew rate on the prototype is not a full 150 V/cycle. Under certain conditions, i.e., a decreasing ramp with high voltage on the load, the slew rate is less than under other conditions. The low slew rates are caused primarily by problems in the predictor system. Some optimization work needs to be done on the predictor circuitry so that it more correctly predicts over those ranges where it now underpredicts, and the correct gap for the transformer needs to be determined and incorporated into the design.

## 4.6 SWITCHING NOISE

Switching noise with dc inputs is due to a slow decay of output voltage through sensing resistors and through the dead band, followed by an active drive to compensate. The amplitude




a. 1-Hz, 1.5V peak.




b. 1-Hz, 5V peak.

Figure 24. Typical square wave rising edge response.

of switching noise is this expected to be proportional to the size of the dead band, and the frequency is to be determined by experiment, although the frequency is not in general expected to be sharply defined. The waveform is experimentally a sawtooth ripple. The rms value of a sawtooth wave is $1/2\sqrt{3}$ of its peak-to-peak value or 0.289. The noise amplitude is expressed in db down from full amplitude. If the ripple peak-to-peak is measured in $\Delta V$, the noise amplitude is

$$A_N = 20 \log \frac{0.289\ \Delta V}{3,000}$$

Switching noise is calculated for the dc tests from the $\Delta V$ and $\Delta t$ data observed. Noise amplitude and frequency are plotted against dc voltage, for the data available, in Figures 25a and 25b. These plots show that noise amplitude is within the specifications listed in Table 1, i.e., 48 db below full amplitude output for dc signals.

Switching noise for two cross-coupled channels commanded to two different dc voltages is calculated in a similar manner. $\Delta V$ was typically 31 V peak-to-peak in these tests; this value corresponds to -50.6 db below full output. It is of note that when cross-coupled channels are commanded to dc voltages of contrary sign, the correction pulses are coincident, but not of higher amplitude. When the voltages are of the same sign, the correction pulses are not coincident. This is an expected condition, for with voltages of contrary sign the effect of the cross-coupling is to cause the correction pulse of any one channel to cross-couple the other to a voltage closer to that for which a correction pulse is required. Since the time constant of the two channels is similar, any condition in which two independent correction pulses are nearly coincident will tend to lead to a condition in which the next correction pulse on one channel will be just enough to cross-couple the other out of its dead band to cause a pulse on it.

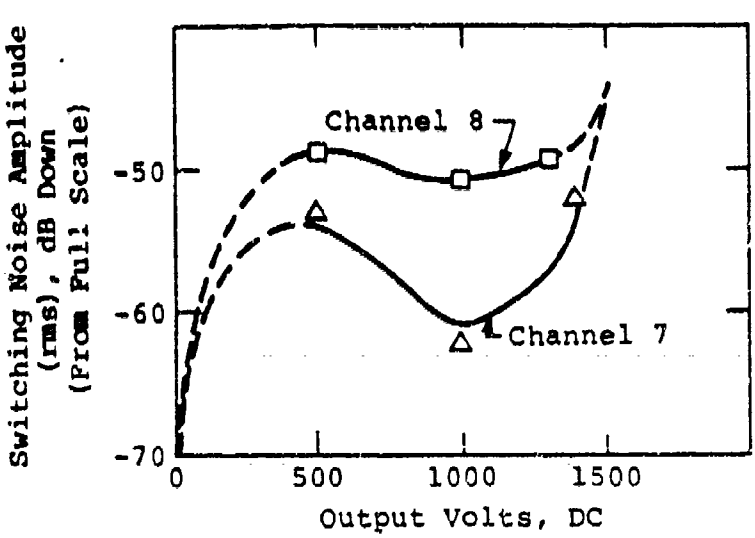



Figure 25a. Switching noise amplitude vs DC voltage.

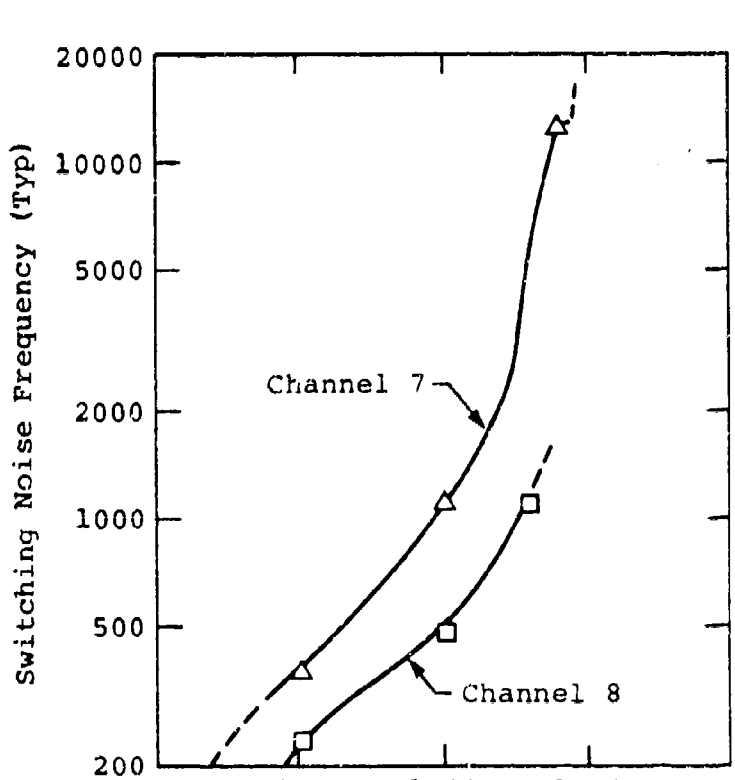



Figure 25b. Switching noise frequency vs DC voltage.

## 4.7 DUAL CHANNEL INTERACTION

Interaction tests, with a 0.01 μf capacitor connected between the high side of the two loads, were performed as listed in Table 4. The dc-dc tests were performed to explore possible switching noise problems. None were seen, as noted above. The dc-sine wave test was performed to study the ability of an amplifier channel to source and sink current from and to an external source. It did so without excessive noise introduced, as is shown in Figure 26. The sine-triangle wave test was performed to search for possible instabilities induced by external sources or sinks. None were observed; Figure 27 is a typical output result.

## 4.8 DRIFT

A drift test was performed on the two channels using a constant input of 6.5 V. In one hour, drift observed was less than one-half percent full scale and may have been as much due to the test instruments as to the actuator amplifiers.

A second drift test, in which measurements were made every five minutes, was terminated just before one hour as a result of the failure of $Q_7$ in channel 7. Time did not permit the test to be repeated. Until the failure, no significant drift was observed.

## 4.9 COMPARISON WITH COMPUTER PREDICTION

It is interesting to compare the output results on a cycle-by-cycle basis to those predicted by the computer program. In Figures 28 and 29 are attempts to do this. Figure 28a is the output of a positive step from -750 V to +750 V--actual data stored on tape and plotted on the X-Y recorder. Figure 28b is the computer program output prediction for a step command from 0 V to 750 V. Figure 29a is actual output for a 1-kHz sine wave signal. Figure 29b represents predicted output for

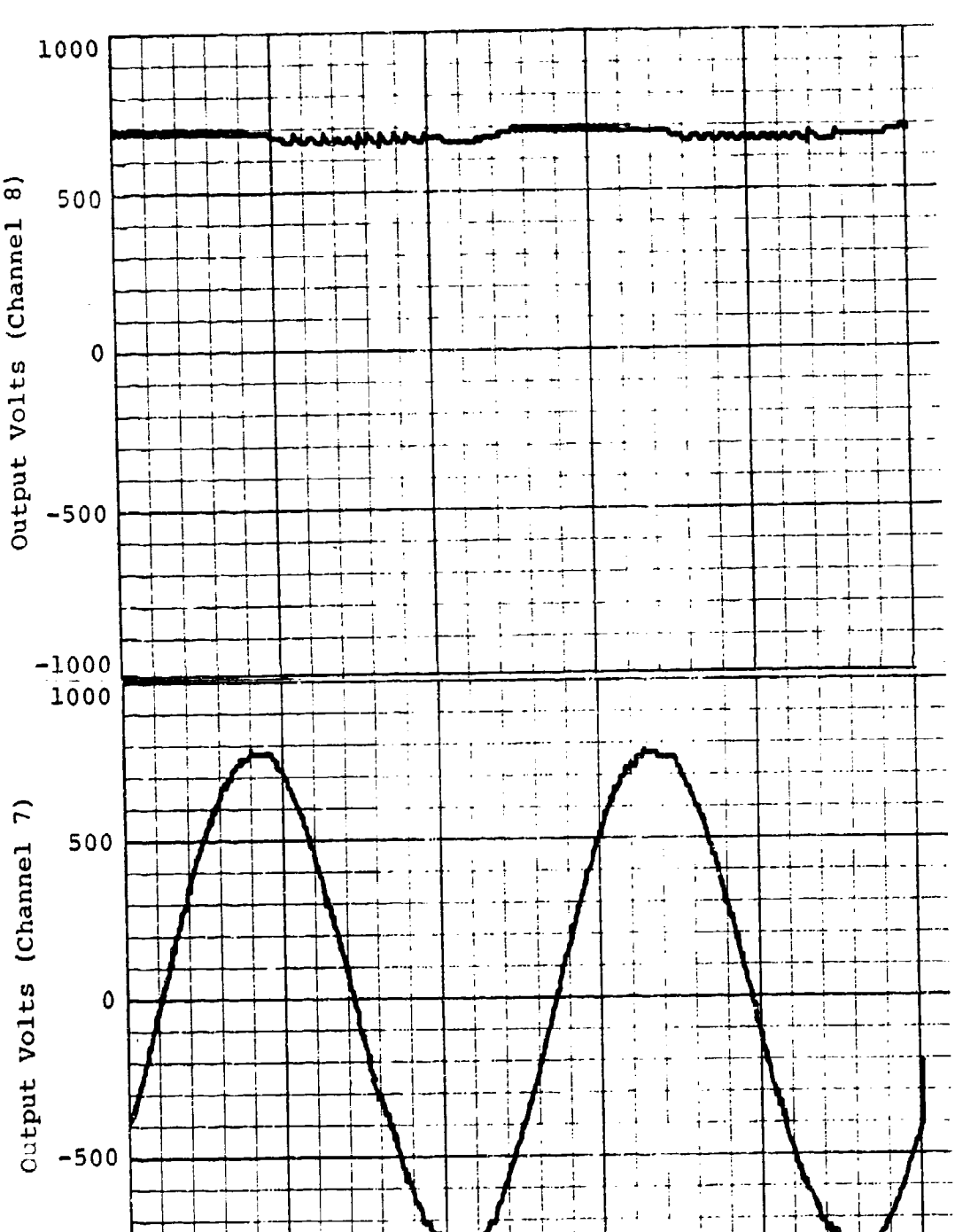



Figure 26. Sine wave vs DC interaction

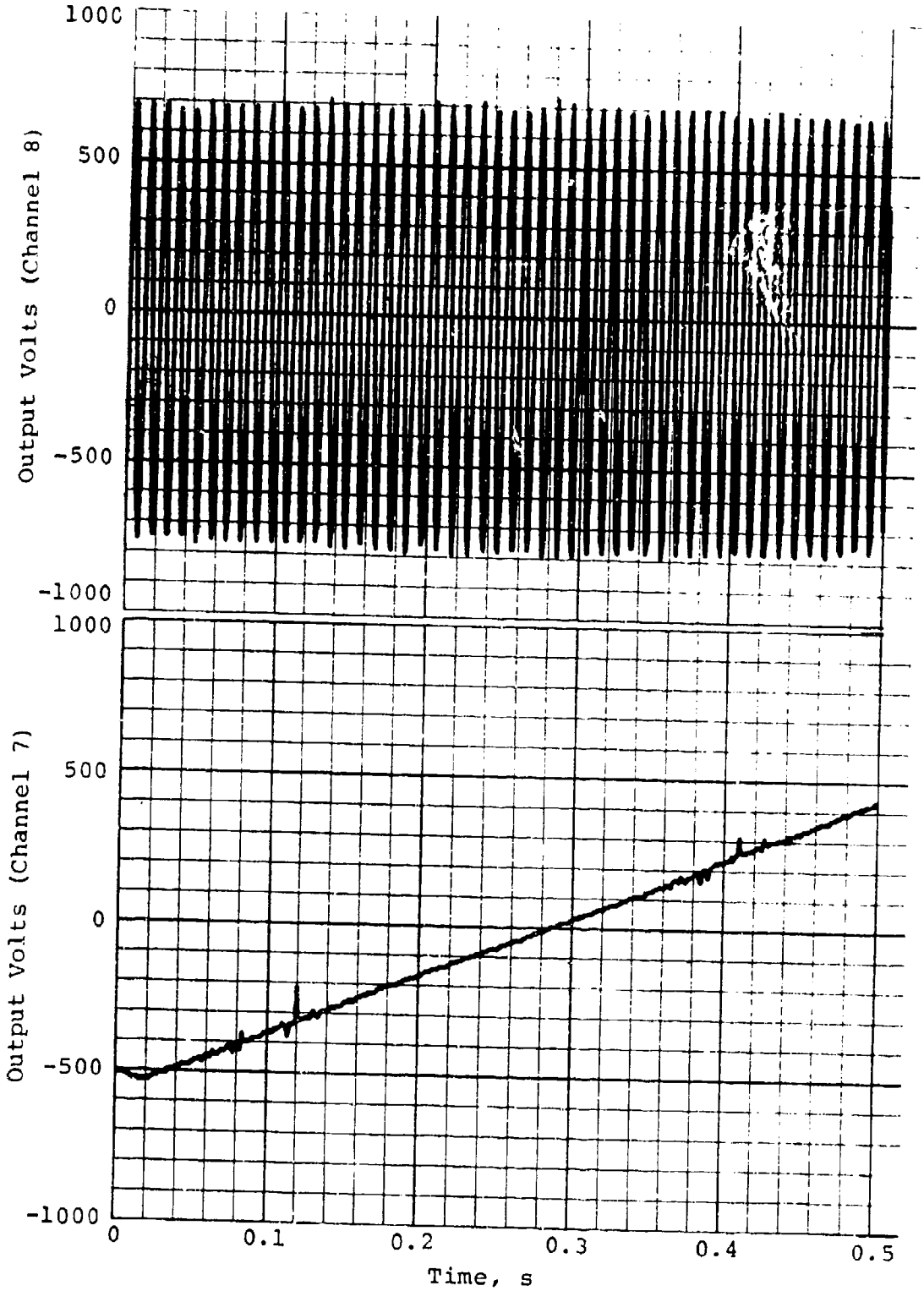
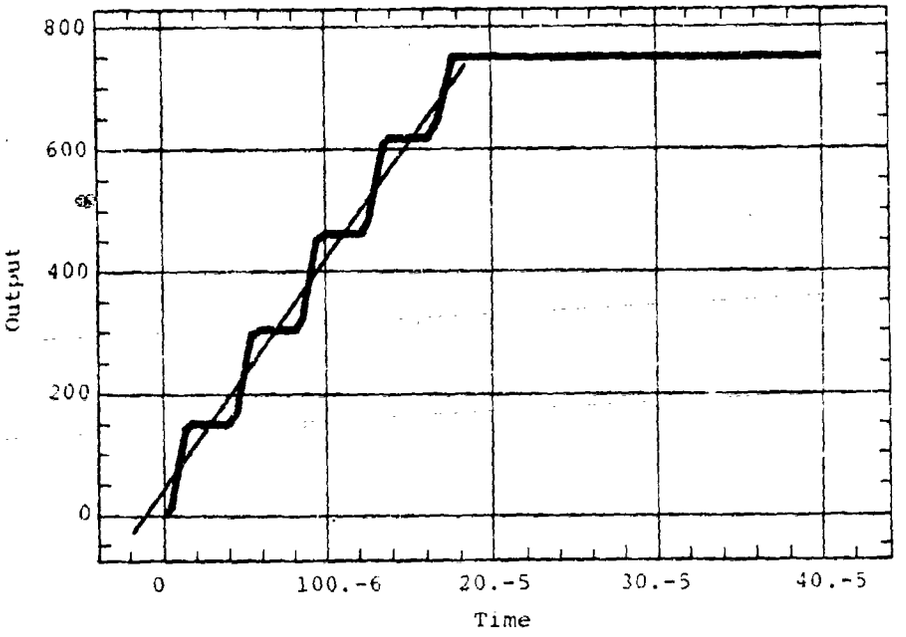



Figure 27. Square wave vs triangular wave.

a.




b.

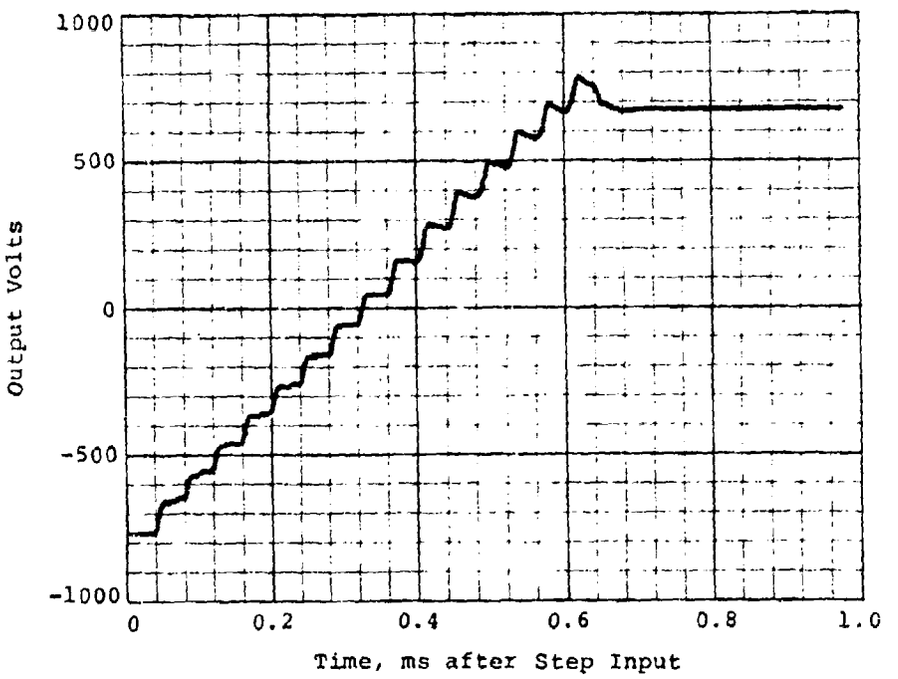



Figure 28. Actual output versus computer model.

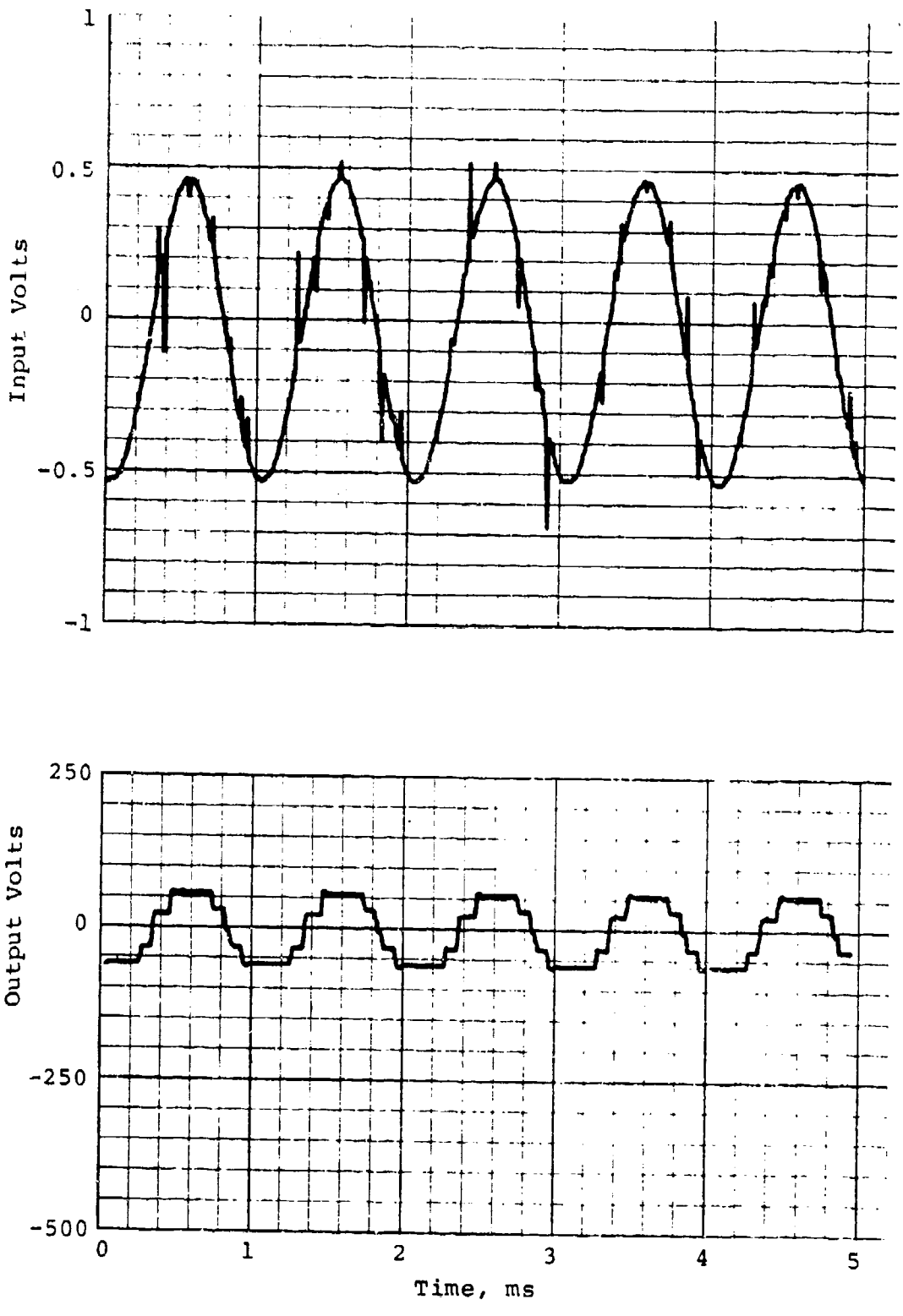



Figure 29a. Actual input and output (0.5 V peak, 1 kH).

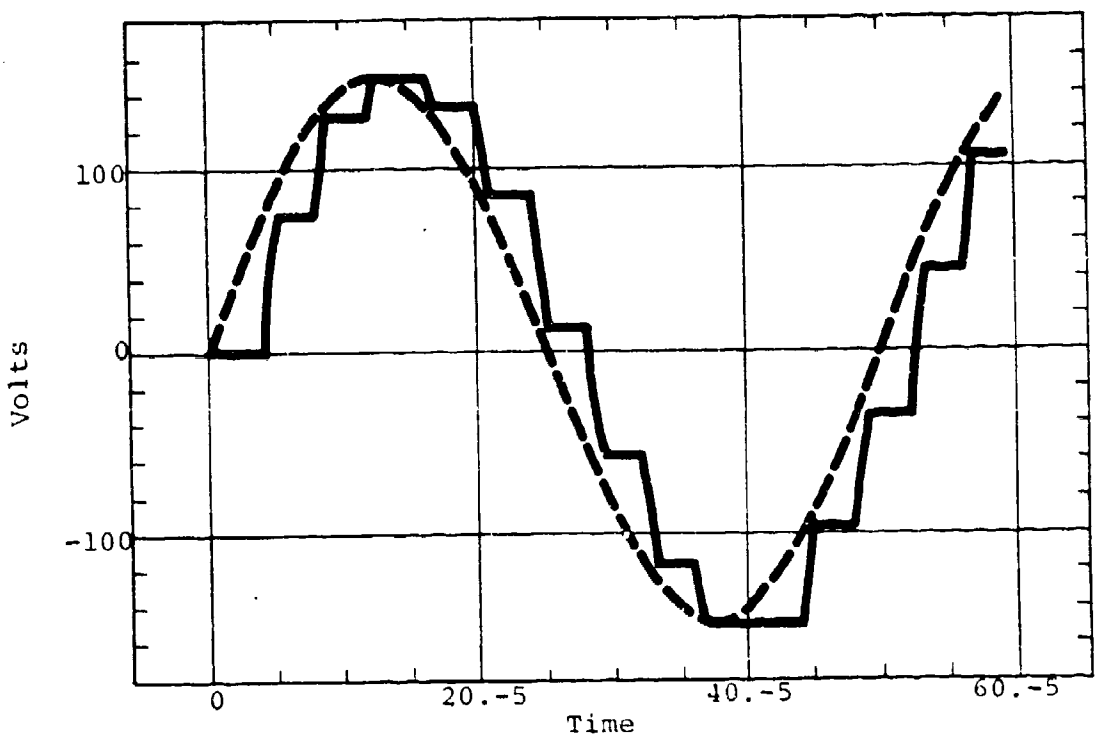



Figure 29b. Computer-predicted output and referenced input (1 V peak, 2 kH). (Compare with Figure 29a.)

a 2-kHz sine wave signal. These comparisons show that the program did produce essentially correct predictions of the amplifier output. (For additional details, see Appendix A.)

Certain features, such as the output setback effect at high voltages seen in Figure 28a, were not predicted by the program because they are caused by effects that the program did not take into account. The setback effect occurs because energy rings through $T_1$ into the capacitance of the HVG devices themselves when the HVG transistors turn off; this energy, stolen from the load, lowers the voltage on it slightly. The effect is considerably greater than first considered during system design, and is presently not compensated by the design of the predictor system. An expanded program such as one based on the alternative state equations in Appendix 1, should predict this effect.

# SECTION 5

# CONCLUSIONS AND RECOMMENDATIONS

The program objective was to develop a design feasible for a 61-channel actuator amplifier system, to build a breadboard to resolve design problems, to perfect the design, and finally to perform specified tests on the breadboard to determine compliance with specifications. The breadboard was in fact a two-channel prototype built to the packaging size constraints that two channels would have in the full system. The two channels were chosen so as to represent a worst case for cross-talk between channels.

In the interest of following a more traditional engineering design approach and to resolve as many questions as possible before constructing a scale prototype, a one-channel breadboard of the power stage was also constructed and used to test components in simulated worst-case circuit conditions. This approach permitted the resolution of basic questions before problems of detail were encountered with the prototype.

These detail problems were resolved, with a few exceptions. The essential design approach has been breadboarded and tested, and shown to meet essential performance specifications. Performance versus design goals is shown in Table 5.

TABLE 5

PERFORMANCE VERSUS DESIGN GOALS

| | Design Goals | Design Achievements As Tested |
|---|---|---|
| Environment | | |
| Altitude | 0-40,000 feet | Not tested |
| Temperature | -65°F - +130°F | Active cooling provided |
| Size and Weight | | |
| Volume | 2 cubic feet | 3 cubic feet |
| Weight | 100 lbs. without coolant | 190 lbs. |
| | 200 lbs. with coolant | <200 lbs. |
| Power Consumption | 10 kw max. | 7.3 kw max |
| Linearity | ±1% | ±<1% except where output signal is slew-rate limited |
| Output Range | -1500 to +1500 V | -1500 to +1500 V on one channel; -1350 to +1350 V on other channel |
| Full Output Swing Frequency Response | dc through 400 Hz | dc through 400 Hz |
| Small Output Swing Frequency Response | dc through 4 kHz | dc through 4 kHz |
| Continuous Adjustment | | |
| Gain | 150 ± 30 | 150 ± 30 |
| Input Offset Constant | ±4 V | ±4 V |
| Fault Protection | | |
| Channel-to-Channel Propagation | | Meets requirements |
| Output Short Circuit | | Meets requirements |
| Input Resistance | 2 kΩ min | 100 kΩ nominal; 2 kΩ for input V >+10 V and <-10 V |
| Input Capacitance | <0.005 μf | <100 pf |
| Input Inductance | <1μH | Within specifications |

The problems of packaging to the given specification have proven considerably more difficult than first anticipated, and some compromise on the size and weight specifications has been necessary. The control approach of predictively solving non-linearly for required time intervals has proven to be a difficult task, not in terms of components or critical tuning, but in terms of comprehensive in -facing and trimming to cover all operating conditions.

At the present time, the ultimate configuration of the mirror actuator system that will use the multi-channel amplifier is not firm. To some extent, the effort remaining to develop a full-scale actuator amplifier depends upon better identification of the application, i.e., number of channels, characteristics of load, etc. Some tasks, however, are common to any configuration and can be pursued in parallel with other system development. Principal efforts of this type are described below.

The efforts fall into three categories: (1) correcting those deficiencies of design or implementation necessary to achieve design goals for voltage and slew rate; (2) improving the design for greater reliability, lower unit cost of channel amplifiers in a full system, and improved performance in areas such as power dissipation and switching noise; and (3) accomplishing those items of an integrative or system nature that must be completed prior to construction of a full system. The efforts are summarized in outline form in Table 6.

The first category is comprised of efforts to optimize the design of the channel step-up transformer. A trade-off must be made in the value of magnetizing inductance required to avoid saturation at maximum dc voltage and when doing large steps, while still holding circulating currents, leakage inductance, and losses to a minimum. Further study must be conducted on the necessity of trade-offs in transformer size. Optimization work is also needed in

TABLE 6

RECOMMENDED FURTHER WORK

I. To Achieve Design Goals

- Transformer (saturation problems above ±1100 max steps)
- Power transistor switching time (> 1100 volts & max slew rate)
- HVG-Voltage setback (> 1200 volts)

II. To Improve Design

- Predictor circuit (improve curve fit)
- Replacing flip-flops with gates/memory elements (improve noise tolerance)

III. Prior to Design Release

- Full brass board circuit including power supplies
- Environmental/durability tests
- Cost-weight trade study

the PS transistor driver circuits to balance the turn-on and turn-off time, consistent with secondary breakdown considerations, for proper interfacing with the predictor circuit functions. The high-voltage setback effect needs to be further studied and properly compensated, at least as far as possible with the present predictor circuit.

The second category involves the study of a design for a modified predictor circuit involving a double integrator producing parabola-type curves. This circuit would have fewer parts and be more reliable than the present system. Use of this circuit would also reduce the number of bus lines required from the common logic to each channel. It is believed that such an approach would be easier to interface to the rest of the circuit under all combinations of conditions, and specifically would be easier to compensate for the voltage setback effect. Also in this category is the study of an alternative logic design containing only gates, and no flip-flops in the channel logic. This design would be inherently immune to potential destructive conditions arising from noise glitches.

The third category is comprised of such items as: (1) artwork modifications to incorporate all the changes already made plus those dictated by the above work; (2) detail design and breadboarding of the common dc power supply of the system converting 400 Hz aircraft ac into the various dc voltages required; and (3) cost-weight trade studies as may be needed.

If size and weight limitations prove critical to the overall system, some consideration should be given to hybridization. However, since the true system requirements are at present unknown, no effort has been made to estimate the volume or weight reduction possible.

Before proceeding with a full-scale multi-channel system, a common power supply should be designed, built, and tested. This element was not required for laboratory testing of a two-channel prototype.

The design fabricated and tested under this contract is a feasible approach to the development of a compact, lightweight, and efficient linear amplifier for piezoelectric transducers. The principal problems of such a circuit have been encountered and solved; the remaining effort required consists of improving reliability and correcting minor design deficiencies.

# APPENDIX A

# AFASEC CIRCUIT ANALYSIS PROGRAM

The theoretical performance of the 61-channel amplifier has been analyzed by means of a computer program (AFASEC) containing: (1) a set of coupled differential equations representing the power switching stage; (2) a representation of the load; (3) algebraic and differential equations representing the channel and control logic; and (4) programming effecting the time-domain solution of these equations.

AFASEC also contains features necessary to make it capable of studying the interrelationships of the parameters that might be varied in design analysis, such as passive component values, turn ratios, clock rates, and load capacitances. There are features for retaining, displaying, and changing these parameters, and for storing them along with single-value output results in a parameter pool on a floppy disk. For each run with given parameters over a given interval of time, the time-domain solutions themselves can be stored on the floppy disk and identified via a directory. They can be tabulated and plotted either on a Tektronix 4010 graphics terminal or on an incremental plotter. Tabulations can also be made of the parameter pool, which is built up from successive runs. Finally, selected parameters of the pool can be plotted against one another.

A listing of the complete program, written in Fortran for the Modcomp III computer with appropriate peripherals, appears in ANNEX 1 of this Appendix.

The program is best understood by noting that the differential equations (lines 348 to 353) and the logic equations (lines 295 to 330) are the "heart" of the program. Surrounding

this heart is a level of programming effecting and managing the time-domain solution of these equations and the compiling of salient parameters (lines 256 through 420). Surrounding this, in turn, is a level of programming providing the working and managing features described above. Statements 790 to the end of the program are specifically dedicated to the graphics facilities required of the Tektronix terminal and the incremental plotter.

To generate the set of coupled differential equations representing the power switching stage, the significant elements of the power circuit are first transformed into an analyzable equivalent circuit, from which loop current equations can be written (Figure A-1).

Central to these transformations is the conversion of the transformer to its T-model equivalent (Figure A-2). A tapped primary can be treated by considering the tap as the bottom end of one winding and the top end of another, and considering one of the windings a secondary. Then two circuits are considered, one for each "secondary" with the other ignored. Finally, the two converted circuits are combined, as shown. In each case it is necessary to common the low end of primary and "secondary" and to perform whatever interchanges in the series layout of elements in the loops (reversal of polarities, etc.) as may be necessary. Where a turns ratio N exists between primary and secondary, voltages, currents, resistances, inductances, and capacitances in the secondary loop must be "referred to the primary," i.e., multiplied or divided by N or $N^2$ as appropriate.

In the simplified equivalent circuit derived in Figure A-1, the tapped primary is considered equivalent to a single primary with a reversible source; that is, the free-wheeling process involving the diode opposite the power transistor is considered

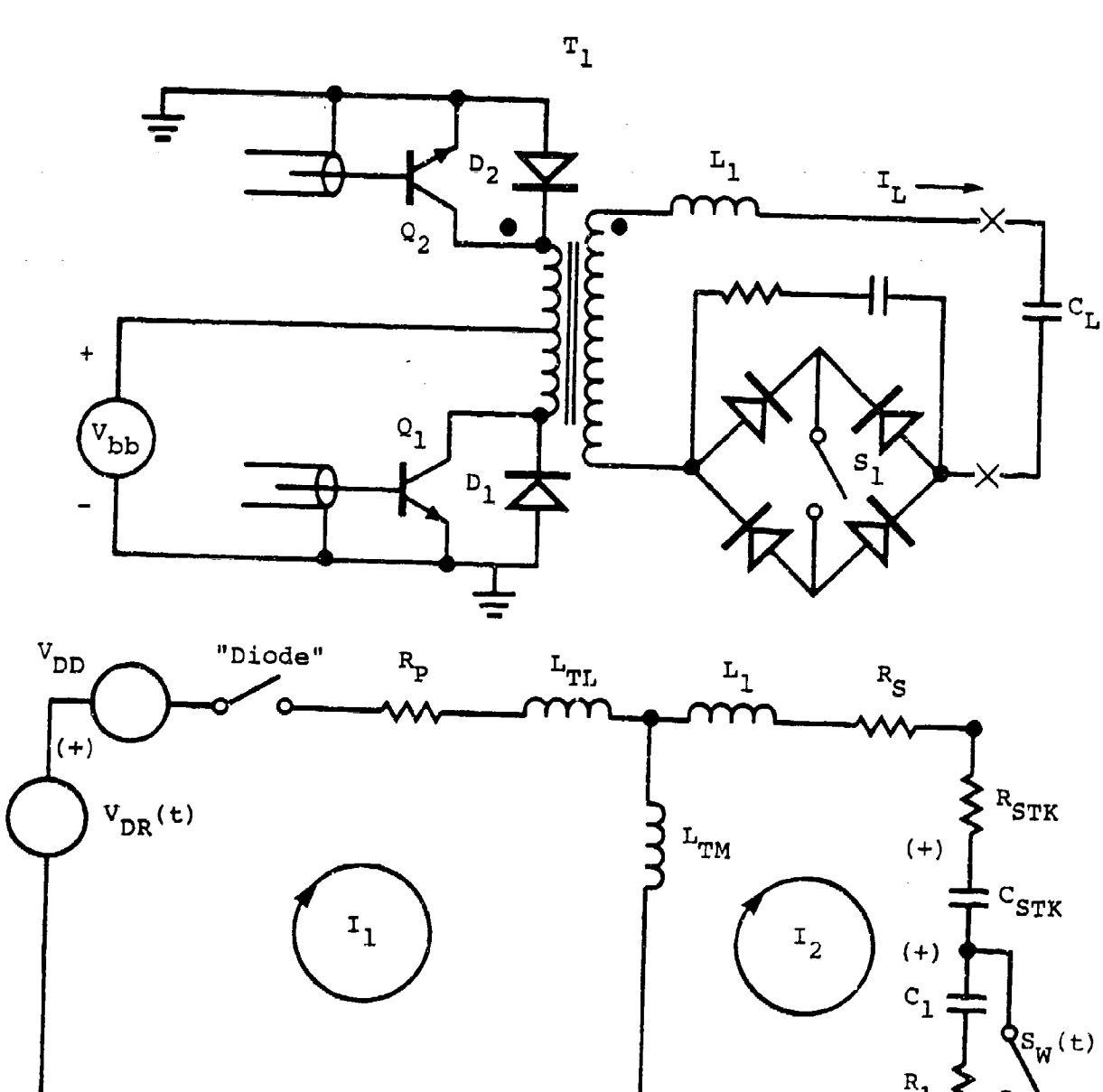



Figure A-1. Conversion of simplified power circuit into analyzable circuit for loop current equations.

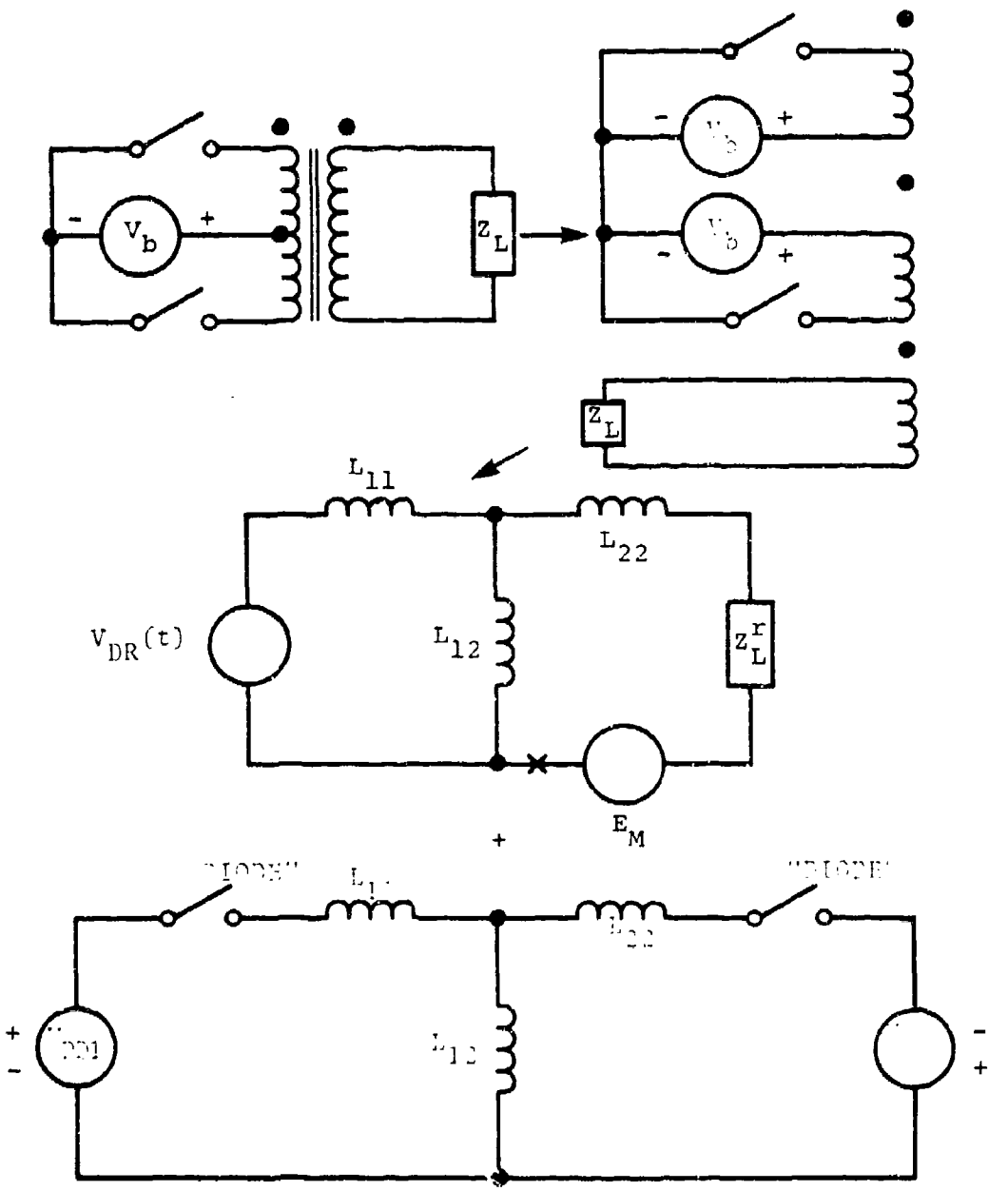



Figure A-2 Methods of deriving an analyzable equivalent circuit of the transformer circuit.

to be the equivalent of a reversal of power source polarity. This approximation ignores the capacitance inherent in the transistors, diodes, and transformer winding. Likewise, in this transformation, the diode quad and HVG is considered a simple switch, and the capacitance of the HVG transistors is ignored.

It is necessary to include a "diode" in the primary current loop of the equivalent circuit to represent the actions of the real diodes of the circuit. This diode is effectively a switch that opens whenever current contrary to the intended direction in any given clock cycle tries to flow. Thus, if at the beginning of a clock period, $Q_1$ (Figure A-1) were to turn on, positive $I_1$ and positive $V_{DR}$ would prevail. The action of $Q_1$ turning off, causing current to free-wheel through $D_2$, would be the equivalent of $V_{DR}$ reversing polarity; however, positive $I_1$ would continue, although decreasing in magnitude. At the instant that the current crosses zero and tries to flow negative, the switch will open to prevent negative current; thus it acts as a "diode." If, on the other hand, $Q_2$ were to turn on, negative $I_1$ would flow at the outset, and the function of the "diode" would be to prevent positive current from flowing at the end of the free-wheeling process. The voltage drop across the real diodes in the circuit, or switching transistors when on, is modeled by a second voltage "source" $V_{DD}$ of a polarity opposite the first source, so it is always dissipating power when current is flowing through it.

In a similar manner a switch is included in the secondary current loop that represents the diode quad and HVG transistors. This switch closes at the outset of any clock cycle in which $Q_1$ or $Q_2$ turns on. The switch opens when the secondary current $I_2$, having increased to a maximum and decreased in a given polarity, tries to reverse polarity.

These switches are represented in the equations as switch functions $\delta$ and $\sigma$, equal either to unity or to zero depending on the state of the switch.

The loop equations for the equivalent circuit of Figure A-1 are:

$$(R_p + sL_{TL} + sL_{TM})\ \delta I_1 - sL_{TM} I_2 = V_{DR} - V_{DD} \qquad (1)$$

$$\left(sL_1 + sL_{TM} + R_s + R_{stk} + \frac{1}{sC_{stk}}\right) I_2 + \left(\frac{1}{sC_1} + R_1\right)\sigma I_2 - sL_{TM}\delta I_1 = 0 \qquad (2)$$

where s is the complex frequency variable, $\delta$ is the "diode" switch function, and $\sigma$ is the HVG switch function.

To effect the Euler's method of solution as used in the program, the equations must be solved for $sI_1$ and $sI_2$, e.g., the highest derivative of the variables. Doing so yields

$$sI_1 = \frac{-(R_s+R_{stk})I_2 - \sigma\left(R_1 I_2 + \frac{\hat{I}_{1s}}{C_1}\right) - \frac{\hat{I}_2}{C_{stk}} - \frac{L_1+L_{TM}}{L_{TM}}(R_p I_1 - V_{DR} + V_{DD})}{\alpha} \qquad (3)$$

$$sI_2 = \frac{\delta(V_{DR}-V_{DD}-R_p I_1) - \frac{L_{TM}+L_{TL}}{L_{TM}}\left[(R_s+R_{stk})I_2 + \frac{\hat{I}_2}{C_{stk}} + \sigma\left(R_1 I_2 + \frac{\hat{I}_{2s}}{C_1}\right)\right]}{\alpha} \qquad (4)$$

where

$$\alpha = \frac{(L_{TM} + L_{TL})\ (L_{TM} + L_1)}{L_{TM}} - L_{TM}$$

and $\hat{I}_2$ and $\hat{I}_{2s}$ represent the integrated $I_2$, causing voltage to accumulate across the capacitors $C_{stk}$ and $C_1$ respectively. As

such, they can be considered independent variables, related by the definition of capacitance

$$I_2 = C_{stk}\, s\hat{I}_2 \tag{5}$$

for $C_{stk}$, and

$$I_2 = C_1 s\hat{I}_{2s} \tag{6}$$

for $C_1$, since $I_2$ is passing through $C_1$ only when the switch is open. When the switch is closed, the voltage on $C_1$ decays through $R_1$, so that when $\sigma$ is zero we have:

$$C_1 \sigma s\hat{I}_{2s} = \frac{\hat{I}_{2s}}{R_1} \tag{7}$$

This equation has an independent time-domain solution.

Equations (3) through (7) can thus be considered the (first-order) state differential equations of the power switching stage.

Equations (3) and (4) are translated to Fortran and appear in the program (lines 348 to 353). The switch functions, $\sigma$ and $\delta$, appear as subroutines, $Q_3$ and DIOD. These subroutines when executed return either the value of their first argument or zero, depending on the state of their other arguments, which in turn determine the state of the switch. Also, the values of components in the program are carried at their actual value rather than at their referred-to-primary value, so it is necessary to multiply or divide them by $N^2$, the square of the turns ratio (ANTR2 in Fortran). Equations (5) and (6) do not appear directly, but the Is are obtained from the sIs by the Euler integration process (lines 342 through 345 and 355 through 359); likewise, the $\hat{I}$s are obtained from the Is. In this process, Equation (7) is also implemented (lines 346 and 360).

Experience gained with the breadboard and the prototype has suggested that certain assumptions made to simplify the equivalent circuit and the differential equations used to model it should not have been made. Figure A-3 illustrates a more comprehensive equivalent circuit. The transformer is modeled by taking its tapped primary as equivalent to a primary and "secondary" (Figure A-2). $L_{TL1}$ and $L_{TL2}$ are equal but separate leakage inductances. Likewise $R_{P1}$ and $R_{P2}$ are equal but separate. The capacitances of the PS transistors and varistors, and primary end-to-end capacitance are included as two lumped components $C_{S1}$ and $C_{S2}$; these may be specified nonlinearly if desired. The capacitance of the HVG transistors and the $T_1$ primary-to-secondary capacitance (see Figure 8) are lumped into a new component $C_{HVG}$. There is another "diode" representing the actions or the diode quad when the transistors are off. The loop current equations are:

$$(R_{P1}+sL_{TL1}+sL_{TM})(\delta_1 I_1+I_3) + sL_{TM}(\delta_2 I_2 + I_4 - I_5) = V_{BB} - V_{DD} \quad (8)$$

$$(R_{P2}+sL_{TL2}+sL_{TM})(\delta_2 I_2+I_4) + sL_{TM}(\delta_1 T_1 + I_3 - I_5) = V_{DD} - V_{BB} \quad (9)$$

$$\frac{I_3}{sC_{s1}} + (R_{P1}+sL_{TL1}+sL_{TM})(\delta_1 I_1+I_3) + sL_{TM}(\delta_2 I_2 + I_4 - I_5) = 0 \quad (10)$$

$$\frac{I_4}{sC_{s2}} + (R_{P2}+sL_{TL2}+sL_{TM})(\delta_2 I_2+I_4) + sL_{TM}(\delta_1 I_1 + I_3 - I_5) = 0 \quad (11)$$

$$\left(R_s + R_{stk} + \frac{1}{sC_{stk}} + sL_1\ sL_{TM}\right) I_5 + \frac{\sigma\ \delta_3}{sC_{HVG}}(I_5 - I_6)$$

$$+ sL_{TM}(\delta_1 I_1 + \delta_2 I_2 + I_3 + I_4) = 0 \quad (12)$$

$$\sigma\left(R_1 + \frac{1}{sC_1}\right) I_6 + \frac{\sigma\ \delta_3}{sC_{HVG}}(I_6 - I_5) = 0 \quad (13)$$

where:

$\delta_1$ is the diode-switching action of $Q_1$ and $D_1$,

$\delta_2$ is the diode-switching action of $Q_2$ and $D_2$,

$\delta_3$ is the diode-switching action of the diode quad when the HVG is open, and

$\sigma$ is the switching action of the HVG, all of these factors equal to unity or zero as appropriate.

When the HVG is closed, $I_6$ is governed by the independent action of $R_1$ and $C_1$,

$$C_1 \, sI_6 = \frac{I_6}{R_1} \tag{14}$$

as in the above set.

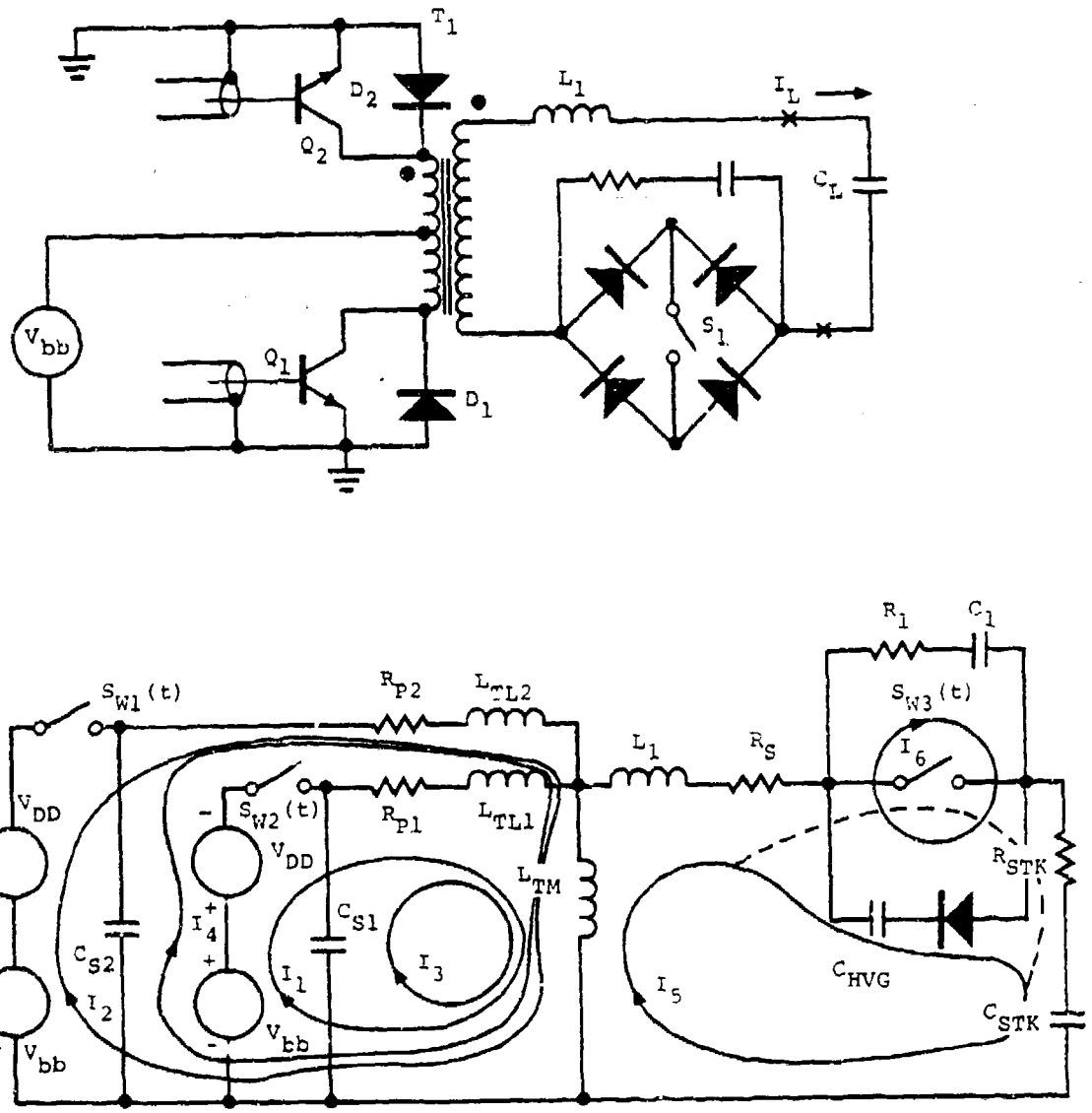



Figure A-3. Expanded conversion of simplified power circuit into analyzable circuit.

```
C    * * A F A S E C * * AIR FORCE ACTUATOR AMPLIFIER SYSTEM EFFICIENCY CALCUL*NS
C     & & HIGH VOLTAGE TRANSISTOR VERSION & & CURRENT ZERO-CROSSING TRANSISTOR
       PROGRAM AFASEC
C    COMT PULSE TURN OFF
C    I/O ASS REQD: 1 = ATO; PLT= CCP, 4 = LP2, 5 = FLOPPY
       INTEGER FENTAV, FENTUD, DRCSSG(30),DRCTRY(5,30)  ,SEDRCY
       DOUBLE PRECISION CBIAS
       LOGICAL XSCAUT,XGRAUT,XLOG,YSCAUT,YGRAUT,YLOG,PPTA,TOK,Q3OFF,DIVF
       LOGICAL PLTMOD(6),POS
       DIMENSION TRCAR(100,7),PARPOL(48),PARI(30),ANPARI(30),ANPR(48),
      *ANMOD(11),LINOPT(5),TIT(13),XLAB(4),YLAB(4),IDRCSSG(30),CVAL(9),
      *ANPARP(20),PVAL(5) ,PLLBSZ(3),PLIMA(8),JUF8(4),JTR(5),JCON(9),
      *AIO(5),AIA(5),SIB(3),AIE(5),AIM(5),SIO(3),SI(3),SIA(3),RCR(20),
      *CXYP(2,50),NGRTA(4),PARLAB(8),JPV(50)
       COMMON/PLOTMU/FMAR,RMAR,BMAR,TMAR  ,XMIN,XMAX,YMIN,YMAX,XSCF,
      *YSCF,XSCAUT,XGRAUT,XLOG,YSCAUT,YGRAUT,YLOG,NPLOVC,XLP(6),YLP(6),
      *XLV(6),YLV(6),NGRDX,NGRDY,NTICX,NTICY,SCRSIZ(4)
       COMMON/PARICO/DT,TF,DTMIN,ANDTP,ANDTC,ANTR,CS,RSTK,ALTS,AL1,AL2,
      *RP,RS,C1,VDD,RWTX,VBB,TDC,VSNM,RRA,AMI,VSO,RWSCR,VIO,Q3OF,DVIM,
      *RC1,FI,TCMS,TCME,PARO(16)
       COMMON/CBDROP/LCB(3),JF
       EQUIVALENCE (TRCAR(1,1),PARPOL(1)),(PLTMOD(1),XSCAUT),(NGRTA(1),
      *NGRDX),(ANPR(1),ANPARI(1)),(PARO(9),WL1),(PARO(10),WL2),
      *(PLLBSZ(1),TITSIZ),(PLLBSZ(2),XLSIZ),(PLLBSZ(3),YLSIZ),(PLIMA(1),
      *FMAR),(AIO(4),ZI20),(AIO(5),ZI30),(PARI(1),DT),(TRCAR(1,4),
      *CXYP(1,1)),(TRCAR(1,5),JPV(1)),(PARLAB(1),ANPR(31))
       DEFINE FILE 5(340,200,U,ICU)
       DATA FENTAV,FENTUD,NPPE,JBLK/1,0,0,2H  /,  DRCSSG/2,3,4,5,6,7,8,9,
      *10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,0/
       DATA JRISE,JTRNON,Q3OFF,PPTA,TOK,POS/2*-1,4*.FALSE./, ALTL,ERTHD,
      *SERTHD/1.E-7,1.E-6,1.E-6/
       DATA ANMOD/44HIP  PP  ST  DI  RU  PL  PR  SP  UP  TE  POS /,ANPR/
      *192HDT  TF  DTMNNDTPNDTCNTR CSTKRSTKLTM L1  L2  RP  RSECC1  VDD RW
      *TXVBB TDC VSNMRRA MI  VSO RWSCVIO Q3OFDVIMRC1 FI  TCMSTCMEVSTKIPRI
      *ISEC    VI  VTR TCUTTOFFWL1 WL2 TVS TIPRTISETISTTVDTTDITEFF WL  /,
      *ANPARP/80HLNOPPMODNGRXNGRYNTCXNTCYTIT TITSXLABXLASYLABYLASFMARRMAR
      *BMARTMARXMINXMAXYMINYMAX/
       DATA RCR/13600.,4500.,2700.,1950.,1360.,1360.,915.,915.,810.,810.,
      *10*620./
       CLKT(T)= DT*ANDTC*40.0*FUNK(T/(DT*ANDTC*40.0))
   10  FORMAT(2H ?,I3)
   11  FORMAT(15H PROGRAM AFASEC)
```

```
      13 FORMAT(A4)
      14 FORMAT(10H ERR NAME )
      16 FORMAT(21H RUN INPUT PARAMETERS/)
      17 FORMAT(2(28X,A4,4X,G10.4/),28H MIN DT VAS-INT CARRIED TO   ,A4,4X,
     *G10.4/28H #DT'S PER PLOT POINT       ,A4,4X,F10.0/11H #DT'S PER ,
     *17HCLOCK COUNT      ,A4,4X,F10.0/,9(28X,A4,4X,G10.4/), 8H DIOD OR,
     *11H XISTR DROP,9X,A4,4X,G10.4/28H JOULES/AMP  XISTR TURNOFF  ,A4,
     *4X,G10.4/28X,A4,4X,G10.4/28H TIME CONST IN VSN CKT      ,A4,4X,
     *G10.4/28H MAX V. VSN CKT CHGD TO     ,A4,4X,G10.4/11H RAMP RATE ,
     *17X,A4,4X,G10.4/28H MODE OF INPUT =1,2,3,4      ,A4,4X,F10.0/28X,
     *A4,4X,G10.4/28H JOULES/VOLT SCR TURNON     ,A4,4X,G10.4/28X,A4,4X,
     *G10.4/28H TIMING FAC FOR Q3 TRNOFF   ,A4,4X,G10.4/12HMI=3,RMPSLP ,
     *16HMI=4,SINWAV AMP ,A4,4X,G10.4/17H R IN SER. W. C1 ,11X,A4,4X,
     *G10.4/20H FREQ.OF INPUT(MI=4),8X,A4,4X,G10.4/,2(28X,A4,4X,G10.4/))
      18 FORMAT(/24H CHANGE? TYPE NAME OR $$)
      19 FORMAT(24H NAME OK. VALUE?(G10.6) )
      20 FORMAT(G10.6)
      22 FORMAT(16H PLOT PARAMETERS/)
      23 FORMAT(5I1)
      24 FORMAT(6I1)
      25 FORMAT(I2)
      26 FORMAT(13A4)
      27 FORMAT(4A4)
      29 FORMAT (32H (I2,5I1,6I1, OR A-FMT AS APPR.) )
      30 FORMAT(16H SORRY NO TRACE.)
      31 FORMAT(19H SORRY FLOPPY FULL.)
      32 FORMAT(20H NAME TRACE FILE(A8))
      33 FORMAT(4A2)
      34 FORMAT(23H STORED - FLOPPY FILE #,I3)
      40 FORMAT(28H SORRY NO DIRECTORY ENTRIES.)
      41 FORMAT(52H ***** T R A C E   F I L E   D I R E C T O R Y *****//
     *23H   NAME  # PTS   FILE #/)
      42 FORMAT(1H ,4A2,I5,4X,I3)
      43 FORMAT(/39H DELETE A FILE? TYPE NAME, ELSE HIT CR.)
      44 FORMAT(16H NAME NOT FOUND.)
      45 FORMAT(6H.GONE.)
      50 FORMAT(21H PRINT OUT? YS OR NO:)
      51 FORMAT(14H OK.HERE GOES.)
      52 FORMAT(1H1,25(2H**),31H A F A S E C  R U N  T R A C E ,25(2H**)//
     *7H INPUT:,10G12.4/2(7X,10G12.4/),/23H    JT LDIV            T ,
     *56H       I1       I2       I3    VSTK        DVDT        DIDT,
     *51H  VINPUT      VQ3      VDRV      TCUT         TOFF NC/)
```

```
      53 FORMAT( 2H #,I4)
      54 FORMAT(1H ,2I5,G12.4,3F6.3,F8.1,2G12.4,F6.3,2F9.1,2G12.4,I3)
      55 FORMAT( 7H DONE. ,I3,30H POINTS STORED. MAX ABSOLUTES:/1H ,A4   ,
     *F10.2,10H AT TIME  ,G10.4/5(1H ,A4,G12.3,10X,G10.4/),
     *2(1H ,A4,G12.4/),
     *11HENERGY OUT:,G10.4,4H IN:,G10.4,6H EFFY:,F8.4/,
     *6H WL1= ,G10.4/6H WL2= ,G10.4/6H WL3= ,G10.4/6H WL4= ,G10.4/
     *6H WL5= ,G10.4/6H WL6= ,G10.4/)
      60 FORMAT(39H SELECT: 1,PLOT FROM CURRENT TRACE MAT /,8X,
     *30H 2,PLOT FROM STORED TRACE MAT /8X,22H 3,PLOT FROM PAR POOL. )
      61 FORMAT(I1)
      62 FORMAT(23H SORRY TRACE MAT NO GO.)
      63 FORMAT(15H SPECIFY TRACE ,I1,33H: 1=IPRI, 2=ISEC, 3=WLOS, 4=VSTK,,
     *21H 5=VIN, 6=VTR , 7=VI  )
      64 FORMAT(15H NAME ABSCISSA.)
      65 FORMAT(19H NOW NAME ORDINATE.)
      66 FORMAT(48H SPECIFY NUMBER OF CONSTANTS FOR SCREENING.(I1) )
      67  FORMAT(15H NAME CONSTANT ,I1)
      69 FORMAT(20H NOW NAME PARAMETER.)
      70 FORMAT(47H SPECIFY # OF VALUES AND THE VALUES.(I1,5G10.6))
      71 FORMAT(I1,5G10.6)
      72 FORMAT(25H SORRY NO POINTS TO PLOT.)
      73 FORMAT(42H SPECIFY PLOTTING DEVICE: 1=ATO, 2=CALCOMP )
      74 FORMAT(24H SORRY NOTHING TO PRINT.)
      75 FORMAT(1H1,23(2H**),37H A F A S E C   T R A C E   A R R A Y ,
     *24(2H**)//8X,4HTIME,8X,4HIPRI,8X,4HISEC,8X,4HWLOS,8X,4HVSTK,8X,
     *4HVIN,8X,4HVTR , /)
      76 FORMAT(1H ,8G12.4)
      77 FORMAT(1H1,22(2H**),42H A F A S E C   P A R A M E T E R   P O O L,
     *22(2H**)//)
      78 FORMAT(3H    ,I2,10G12.4/4(6X,1 G12.4/)/)
      79 FORMAT(7H DONE. )
      80 FORMAT(21H SORRY PAR POOL FULL.)
      90 FORMAT(44H UPDATE PAR POOL. SPECIFY WHICH RECORD.(I2) )
      91 FORMAT(/A1,A4,G12.4/))
      94 FORMAT(46H SPECIFY # OF VALUES AND LIMITS (I1,2G10.6)     )
      99 FORMAT(5H BYE   )
C
C   ##S T A R T   O F   P R O G R A M###
C
        WRITE(1,11)
        READ(5'1)(PARI(J),J=1,30),INPPE,XSCAUT,XGRAUT,XLOG,YSCAUT,YGRAUT,
```

```
     *YLOG,NGRDX,NGRDY,NTICX,NTICY,(LINOPT(K),K=1,5),TITSIZ,XLSIZ,YLSIZ,
     *FMAR,RMAR,BMAR,TMAR,XMIN,XMAX,YMIN,YMAX,(TIT(L),L=1,13),(XLAB(M),
     *M=1,4),(YLAB(N),N=1,4)
      READ(5,2)((DRCTRY(JA,J8),JA=1,5),J6=1,30),(IDRCSSG
     *(JC),JC=1,30),IFENTAV,IFENTUD,JFITST
      IF(JFITST.NE.-12345) GO TO 95
      NPPE = INPPE
      FENTAV = IFENTAV
      FENTUD = IFENTUD
      DO 93 J = 1,30
   93 DRCSSG(J)= IDRCSSG(J)
   95 WRITE(1,10) NPPE
      MD = JEPARN(ANMOD)
      GO TO (100,200,300,400,500,600,700,800,900,990,950),MD
C
C    ## IP - INPUT RUN PARAMETERS, DISPLAY AND CHANGE ##
C
  100 CALL BLANK
      WRITE(1,16)
      WRITE(1,17)(ANPARI(J),PARI(J),J=1,30)
  102 WRITE(1,18)
      NAPAR = JEPARN(ANPARI)
      IF(NAPAR)109,109,104
  104 WRITE(1,19)
      READ (1,20) PARI(NAPAR)
      GO TO 102
  109 CALL BLANK
      WRITE(1,16)
      WRITE(1,17)(ANPARI(J),PARI(J),J=1,30)
      GO TO 95
C
C    ## PP - PLOT PARAMETERS, DISPLAY AND CHANGE ##
C
  200 CALL BLANK
      WRITE(1,22)
      CALL WPLPAR(ANPARP,LINOPT,TIT,XLAB,YLAB,PLLBSZ)
  202 WRITE(1,18)
      NAPAR = JEPARN(ANPARP)
      IF(NAPAR) 219,219,204
  204 WRITE(1,19)
      WRITE(1,29)
      GO TO(205,206,207,207,207,207,208,209,210,209,211,209,212,212,212,
```

```
      *212,212,212,212,212),NAPAR
  205 READ(1,23)(LINOPT(J),J=1,5)
      GO TO 202
  206 READ(1,24)(IDRCSSG(J),J=1,6)
      DO 226 J = 1,6
      PLTMOD(J) = .FALSE.
      IF(IDRCSSG(J).EQ.1) PLTMOD(J) = .TRUE.
  226 CONTINUE
      GO TO 202
  207 READ(1,25) NGRTA(NAPAR-2)
      GO TO 202
  208 CALL CLRBUF(TIT(1),26)
      READ(1,26)(TIT(J),J=1,13)
      GO TO 202
  209 READ(1,20) PLLBSZ(NAPAR/2-3)
      GO TO 202
  210 CALL CLRBUF(XLAB(1),8)
      READ(1,27)(XLAB(J),J=1,4)
      GO TO 202
  211 CALL CLRBUF(YLAB(1),8)
      READ(1,27)(YLAB(J),J=1,4)
      GO TO 202
  212 READ(1,20)PLIMA(NAPAR-12)
      GO TO 202
  219 CALL BLANK
      WRITE(1,22)
      CALL WPLPAR(ANPARP,LINOPT,TIT,XLAB,YLAB,PLLBSZ)
      GO TO 95
C
C   ## ST - STORE TRACE AND UPDATE DIRECTORY ##
C
  300 IF(TOK) GO TO 302
      WRITE(1,30)
      GO TO 95
  302 IF(FENTAV.GT.0) GO TO 304
      WRITE(1,31)
      GO TO 95
  304 N= FENTAV
      FENTAV = DRCSSG(N)
      DRCSSG(N) = FENTUU
      FENTUU = N
      CALL CLRBUF(DRCTRY(1,N),4)
```

```
      WRITE(1,32)
      READ(1,33)(DRCTRY(J,N),J=1,4)
      DRCTRY(5,N)=NPTS
      J = 93+N*8
      DO 306 L = 1,7
      K = J - 1 + L
  306 WRITE(5'K)(TRCAR(M,L),M=1,100)
      WRITE(1,34) J
      GO TO 95
C
C   ## DI - LIST DIRECTORY AND DELETE ENTRIES
C
  400 IF(FENTUD.GT.0) GO TO 402
      WRITE(1,40)
      GO TO 95
  402 CALL BLANK
      WRITE(1,41)
      N = FENTUD
  404 WRITE(_,42)(DRCTRY(J,N),J=1,5), N
      N = DRCSSG(N)
      IF(N) 405,405,404
C                 NOW TO DELETE ENTRIES
  405 WRITE(1,43)
      CALL CLRBUF(JUF8(1),4)
      READ(1,33)(JUF8(J),J=1,4)
      IF(JUF8(1).EQ.JBLK) GO TO 95
      N = SEDRCY(JUF8,DRCSSG,FENTUD,DRCTRY)
      IF(N.GT.0) GO TO 407
      WRITE(1,44)
      GO TO 405
  407 DO 408 J = 1,30
      IF (DRCSSG(J).EQ.N) GO TO 409
  408 CONTINUE
  409 DRCSSG(J) = DRCSSG(N)
      DRCSSG(N) = FENTAV
      FENTAV = N
      WRITE(1,45)
      GO TO 405
C
C   ##RU - RUN CIRCUIT MODEL ##
  500 CALL BLANK
      WRITE(1,50)
```

```
      READ(1,33) JP
  501 WRITE(1,51)
C                 INITIAL CONDITIONS & PRE-COMPUTE CONSTANTS
      DO 502 J = 1,10
  502 PARO(J) = 0.
      WO = 0.0
      WL3 = 0.0
      WL4 = 0.0
      WL5 = 0.0
      WL6 = 0.0
      DO 504 J = 1,3
      AIO(J) = 0.
  504 SIO(J) = 0.
      ZI20 = CS*VS0*ANTR
      ZI30 = 0.
      NDTC = INT(PARI(5))
      MI = INT(PARI(21))
      VS = VS0
      VI = VI0
      NPTS = 0
      JDRV = 0
      JPCHG = 0
      JTRNON = 0
      Q3OFF = .TRUE.
      JRISE = NULSW(VI-VS/150.,1,-1)
      IF(MI.GE.3.AND.DVIM.GT.0.0) JRISE=1
      JIS = JRISE
      ANTR2 = ANTR**2
      N40NDT = 40*NDTC
      ALFA = (ALTM+ALTL)*(ALTM+(AL1/ANTR2  ))/ALTM - ALTM
      IF(JP.EQ.2HYS) WRITE(4,52)(PARI(J),J=1,30)
C                 MAIN INTEGRATION LOOP
      LT = INT(TF/DT)
      DO 550 JT=1,LT
      NCLK = MOD(JT/NDTC,40)
      IF(NCLK.GE.40) NCLK = 0
      T = DT*FLOAT(JT)
C                 CALCULATE COMMAND VOLTAGE
      IF(MI.EQ.3  ) VI = VI0 + T * DVIM
      IF( MI.EQ.4  ) VI = DVIM * SIN(T*FI*6.28318)
      IF(NCLK.GT.0) GO TO 508
C                 LOGIC EQUATIONS
```

```
      VSC = VS/150.
      VSCA = ABS(VSC)
      VSL = 0.5 * (10.+FLOAT(JRISE)*VSC)
      VSN = VSNM *EXP(-(VSL/(RRA*TDC)))
      VCR = 0.
      VISH = ABS(10.*(VI-VSC))
      IF(VISH.GT.10.0) VISH = 10.0
      IF(VISH.GT.0.6) GO TO 506
      JT = N40NDT - 1 + JT
      GO TO 545
  506 JSP = NOLSW(VSC,1,-1)
      TOFF = 39.0*DT*ANDTC
      JT = NDTC - 1 + JT
      GO TO 545
  508 IF(NCLK.EQ.20) GO TO 510
      IF(AI0(1).EQ.0.0. AND. VCR.GE.VISH .AND. CLKT(T).LT.TOFF) TOFF =
     *CLKT(T)
      JCOMUT = 0
      IF(.NOT.Q3OFF .AND. JSP*JRISE.LT.0 .AND. CLKT(T).GT.TOFF.AND.
     *FLOAT(JRISE)*AI0(2).GT.0.0) JCOMUT = 1
      JDRV = 0
      IF(NCLK.LE.20) VCR = VCR + VSN*DT/(1.0E-9*RCR(NCLK))
      IF(VCR.LT.VISH)JDRV = 1
      GO TO 511
  510 JRISE = NOLSW(VI-VS/150.,1,-1)
  511 VOP = (JDRV*JRISE + JCOMUT*JSP)*(VBB-VDD) - (1-JDRV)*(1-JCOMUT)*
     *JIS*(VBB+VDD)
      IF(JTRNON.EQ.0.AND.( JDRV).GE.1) Q3OFF = .FALSE.
      IF(JTRNON.EQ.0 .AND. (JCOMUT+JDRV).GE.1) JTRNON = 2
      IF(JTRNON.GT.0 .AND. (JCOMUT+JDRV).EQ.0) GO TO 512
      IF(VCR.GE.VISH .AND. FLOAT(JRISE)*AI0(2).LT.0.0) Q3OFF = .TRUE.
      GO TO 513
  512 JIS = NOLSW(AI0(1),1,-1)
      WL1 = WL1 + ABS(AI0(1))*RWTX
      IF(VCR.GE.VISH .AND. CLKT(T).LT.TOFF) TCUT = CLKT(T)
      JTRNON = 0
  513 LDIV = 2
      DIVF = .FALSE.
C                 VARIABLE SUBDIVISION LOOP
  514 CALL ETARA(AIA,AI0,5)
      CALL ETARA(SIA,SI0,3)
      DTO = DT/FLOAT(LDIV)
```

```
      DO 540 KT=1,LDIV
      IF(MOD(KT,2).EQ.0) GO TO 516
      CALL ETARA(SIB,SIA,3)
      NIT = 0
C                 EULER EQUATIONS
  516 DO 518 L = 1,2
  518 AIE(L) = AIA(L) + SIB(L)*DTD
      AIE(4) = AIA(4) + AIA(2)*DTD
      AIE(5) = AIA(5)
      IF(Q30FF) AIE(5) = AIA(5) + AIA(2)*DTD
C             DIFFERENTIAL EQUATIONS
  520 SI(1) = ( - ((AL1/ANTR2 + ALTM    ALTM) * (RP*AIE(1) - VDP)
     * - ((RS + RSTK) * AIE(2) + AIE( )/CS + Q3 (AIE(5)/C1
     * + RC1*AIE(2), Q30FF, AIE(2))) / ANTR2 ) / ALFA
      SI(2) = ( DIOD( (ALTM/(ALTL+ALTM)) * (VDP - RP*AIE(1) ),
     * VDP, JTRNON, AIE(1) ) - ( (RSTK+RS)*AIE(2) + AIE(4)/CS
     * + Q3 (AIE(5)/C1 + RC1*AIE(2), Q30FF, AIE(2)))/ANTR2)/ALFA
C                 MODIFIED EULER EQUATIONS
      AIM(1) = DIOD(AIA(1)+(SIB(1)+SI(1))*DTD/2.0,VDP,JTRNON,AIA(1) +
     *(SIB(1)+SI(1))*DTD/2.0 )
      AIM(2) = AIA(2)+(SIB(2)+SI(2))*DTD/2.0
      AIM(4) = AIA(4)+(AIA(2)+AIM(2))*DTD/2.0
      AIM(5) = AIA(5)+(AIA(2)+AIM(2))*DTD/2.0
      IF(.NOT.Q30FF) AIM(5) = AIA(5) - AIA(5)*DTD/(C1*ANTR*RC1)
C                 EULER ERROR GATE
      DO 522 L = 1,2
      IF((AIM(L)-AIE(L))**2.GT.ERTHD) GO TO 528
  522 CONTINUE
      IF(MOD(KT,2).EQ.0) GO TO 524
      CALL ETARA(SIB,SI ,3)
      GO TO 536
C                 SIMPSON CURVATURE CHECK
  524 DO 526 L = 1,2
      IF((DT*(SIA(L)-2.0*SIB(L)+SI(L)))**2.GT.SERTHD)GO TO 530
  526 CONTINUE
      GO TO 535
C                 EULER WASHOUTS
  528 NIT = NIT + 1
      IF(NIT.GT.8) GO TO 530
      CALL ETARA(AIE,AIM,5)
      GO TO 520
C                 SIMPSON WASHOUTS
```

```
      530 IF(DIVF)GO TO 535
          IF(DTD.LT.DTMIN)GO TO 532
          LDIV = LDIV*2
          GO TO 514
      532 DIVF = .TRUE.
          WRITE(1,53)JT
          GO TO 514
C                   WRAP UP INNER LOOP
      535 NIT = 0
      536 CALL ETARA(AIA,AIM,5)
      540 CONTINUE
          CALL ETARA(AIO,AIM,5)
          CALL ETARA(SIO,SI,3)
C                   WRAP UP OUTER LOOP
          IF(MOD(JT,INT(ANDTP)),NE,0) GO TO 547
      545 NPTS = NPTS + 1
          TRCAR(NPTS,1) = T
          TRCAR(NPTS,2) = AIO(1)
          CALL COUV(AIO,SIO,AI2,Q3OFF,VS,DVDT,VTR)
          TRCAR(NPTS,3) = AI2
          TRCAR(NPTS,4) = WL
          TRCAR(NPTS,5) = VS
          TRCAR(NPTS,6) = VI*150.
          TRCAR(NPTS,7) = VTR
      547 CALL COUV(AIO,SIO,AI2,Q3OFF,VS,DVDT,VTR)
          WO = WO + RSTK*(AI2**2)*DT
          WL3 = WL3 + RP*(AIO(1)**2)*DT
          WL4 = WL4 + RS*(AI2**2)*DT
          WL5 = WL5 + VDD*ABS(AIO(1))*DT
          IF(Q3OFF) WL6 = WL6 + DT*RC1*AI2**2
          WL = WL1 + WL2 + WL3 + WL4 + WL5 + WL6
          IF(JP.EQ.2HYS) WRITE(4,54)JT,LDIV,T,AIO(1),AI2,WL,VS,DVDT,
         *SIO(2),VI,VTR,VOP,TCUT,TOFF,NCLK
          CALL AMXSET(VS,1,T)
          CALL AMXSET(AIO(1),2,T)
          CALL AMXSET(AI2,3,T)
          CALL AMXSET(AI3,4,T)
          CALL AMXSET(VI,5,T)
          CALL AMXSET(VTR,6,T)
          CALL AMXSET(TCUT,7,T)
          CALL AMXSET(TOFF,8,T)
      550 CONTINUE
```

```
      EFF = WO/(WO+WL)
      IF(POS) GO TO 802
      TOK = .TRUE.
      PPTA = .FALSE.
      WRITE(1,55) NPTS,(PARLAB(L),PARO(L),PARO(L+10),L=1,6),(PARLAB(L),
     *PARO(L),L=7,8),WO,WL,EFF,WL1,WL2,WL3,WL4,WL5,WL6
      GO TO 95
C
C   ## PL - P L O T  ##
C
  600 WRITE(1,60)
      READ (1,61) JP
      IF(JP.LE.0.OR.JP.GE.4) GO TO 600
      GO TO(606,602,610),JP
  602 WRITE(1,32)
      CALL CLRBUF(JUF8(1),4)
      READ(1,33)(JUF8(J),J=1,4)
      N = SEDRCY(JUF8,DRCSSG,FENTUD,DRCTRY)
      IF(N.GT.0) GO TO 604
      WRITE(1,44)
      GO TO 600
  604 J = 93 + N*8
      DO 605 L = 1,7
      K = J - 1 + L
  605 READ(5'K)(TRCAR(M,L),M=1,100)
      NPTS = DRCTRY(5,N)
      TOK = .TRUE.
      PPTA = .FALSE.
      GO TO 608
  606 IF(TOK)GO TO 608
      WRITE(1,62)
      GO TO 95
  608 JT = 0
  609 IF(LINOPT(JT+1).EQ.0) GO TO 630
      JT = JT + 1
      WRITE(1,63)JT
      READ (1,61)JTR(JT)
      IF(JT-5) 609,630,630
C                 HERE TO SET UP PLOT FROM PAR POOL
  610 WRITE(1,64)
      NABS = JEPARN(ANPR)
      WRITE(1,65)
```

```
      NORD=JEPARN(ANPR)
      WRITE(1,66)
      READ (1,61)NCON
      DO 614 J = 1,NCON
      WRITE(1,67)J
      JCON(J) = JEPARN(ANPR)
      WRITE(1,19)
      READ (1,20)CVAL(J)
  614 CONTINUE
      WRITE(1,69)
      NAPAR = JEPARN(ANPR)
      WRITE(1,70)
      READ (1,71)NPVAL,(PVAL(J),J=1,5)
      TOK = .FALSE.
      PPTA = .TRUE.
      INPPE = 0
      DO 624 J = 1,NPPE
      K = J + 2
      READ(5*K)(PARPOL(M),M=1,48)
      DO 618 K = 1,NCON
      IF(PARPOL(JCON(K)).NE.CVAL(K))GO TO 624
  618 CONTINUE
      DO 620 K = 1,NPVAL
      IF(PARPOL(NAPAR) .EQ.PVAL(K)) GO TO 622
  620 CONTINUE
      GO TO 624
  622 INPPE = INPPE + 1
      CXYP(1,INPPE) = PARPOL(NORD)
      CXYP(2,INPPE) = PARPOL(NABS)
      JPV (INPPE) = K
  624 CONTINUE
      IF(INPPE) 625,625,626
  625 WRITE(1,72)
      GO TO 95
  626 DO 629 J = 1,INPPE
      D  = CXYP(1,1)
      F  = FLOAT(JPV(1))
      DO 628 K =1,INPPE
      IF(D  .LT.CXYP(1,K))GO TO 628
      D   = CXYP(1,K)
      F   = FLOAT(JPV(K))
      L = K
```

```
      628 CONTINUE
          TRCAR(J,1) = D
          TRCAR(J,2)=CXYP(2,L)
          TRCAR(J,3) = F
          CXYP(1,L) = 1.0E9
      629 CONTINUE
          NPTS = INPPE
          JT = 1
          JTR(1) = 1
C                 NOW FOR THE PLOT
      630 WRITE(1,73)
          READ (1,61)NPLOVC
      634 CALL PEN(0.,0.,-3)
C                 DRAW THE FRAME,GRID LINES AND TICS
          WIDE = SCRSIZ(NPLOVC *2-1)-RMAR
          HIGH = SCRSIZ(NPLOVC*2)-TMAR
          CALL PEN(FMAR,BMAR,3)
          CALL PEN(FMAR,HIGH,2)
          CALL PEN(WIDE,HIGH,2)
          CALL PEN(WIDE,BMAR,2)
          CALL PEN(FMAR,BMAR,2)
          CALL TAXSCN(1,NPTS,1,TRCAR,JTR)
          CALL TAXSCN(2,NPTS,JT,TRCAR,JTR)
C                 DRAW THE LABELS
          IF(XGRAUT)GO TO 638
          CALL BQUL(CBIAS(XMIN),6,FMAR-0.1,BMAR-0.12,0.1,0.)
          CALL BQUL(CBIAS(XMAX),6,WIDE-0.2,BMAR-0.12,0.1,0.)
          GO TO 640
      638 DO 639 J = 1,6
          IF(XLP(J).LT.WIDE)CALL BQUL(CBIAS(XLV(J)),6,XLP(J)-0.16,BMAR-0.12,
         *0.1,0.)
      639 CONTINUE
      640 IF(YGRAUT)GO TO 642
          CALL BQUL(CBIAS(YMIN),6,FMAR-0.02,BMAR,0.1,1.571)
          CALL BQUL(CBIAS(YMAX),6,FMAR-0.02,HIGH-0.2,0.1,1.571)
          GO TO 646
      642 DO 644 J = 1,6
          IF(YLP(J).LT.HIGH)CALL BQUL(CBIAS(YLV(J)),6,FMAR-0.02,YLP(J)-0.16,
         * 0.1,1.571)
      644 CONTINUE
      646 CALL BQUL(XLAB,16,((FMAR+WIDE)/2.0-10.0*XLSIZ),BMAR-0.14-XLSIZ,
         *XLSIZ,0.0)
```

```
      CALL BQUL(YLAB,16, FMAR-0.14,((BMAR+HIGH)/2.0-10.0*YLSIZ),YLSIZ,
     *1.571)
      CALL BQUL(TIT,52,FMAR + 0.2,HIGH+0.04,TITSIZ,
     *0.0)
C                 NOW DRAW THE LINES
  650 IF(PPTA) GO TO 656
      DO 652 J = 1,JT
      CALL PLOTA(NPTS,TRCAR(1,1),TRCAR(1,JTR(J)+1),LINOPT(J),PPTA,D)
  652 CONTINUE
      GO TO 670
  656 DO 660 J = 1,NPVAL
      CALL PLOTA(NPTS,TRCAR(1,1),TRCAR(1,2),LINOPT(J),PPTA,TRCAR(1,3))
  660 CONTINUE
  670 CALL PEN(0.,0.,0)
      READ(1,13) D
C                 WAIT HERE FOR USER TO LOOK HIS PLOT OVER
      GO TO 95
C
C   ## PR - PRINT TRACE ARRAY OR PAR POOL
C
  700 IF(PPTA) GO TO 720
      IF(TOK)  GO TO 710
      WRITE(1,74)
      GO TO 95
  710 WRITE(4,75)
      DO 712 J = 1,NPTS
      WRITE(4,76)  (TRCAR(J,L),L=1,7)
  712 CONTINUE
      GO TO 730
  720 WRITE(4,77)
      DO 722 J = 1,NPPE
      K = J + 2
      READ(5*K)(PARPOL(M),M=1,48)
      WRITE(4,78) J, (PARPOL(L),L=1,47)
  722 CONTINUE
  730 WRITE(4,79)
      GO TO 95
C
C   ## SP - STORE PARAMETERS IN PAR POOL
C
  800 IF(TOK) GO TO 802
      WRITE(1,62)
```

```
589         GO TO 95
590     802 IF(NPPE.LT.338) GO TO 804
591         WRITE(1,80)
592         GO TO 95
593     804 IF(NPPE.EQ.0) GO TO 805
594     805 NPPE = NPPE + 1
595         DO 806 J = 1,30
596     806 PARPOL(J)=PARI(J)
597         DO 808 J = 1,16
598     808 PARPOL(J+30)=PARO(J)
599         PARPOL(47) = EFF
600         PARPOL(48) = WL
601         K = NPPE + 2
602     810 WRITE(5*K)(PARPOL(M),M=1,48)
603         TOK = .FALSE.
604         PPTA = .TRUE.
605         IF(POS) GO TO 956
606         GO TO 95
607   C
608   C   ##  UP - UPDATE PAR POOL
609   C
610     900 WRITE(1,90)
611         READ(1,25) JP
612         K = JP + 2
613         READ (5*K)(PARPOL(M),M=1,48)
614         CALL BLANK
615         WRITE(1,91)(ANPR(J),PARPOL(J ),J=1,48)
616     902 WRITE(1,18)
617         NAPAR = JEPARN(ANPR)
618         IF(NAPAR) 906,906,904
619     904 WRITE(1,19)
620         READ (1,20) PARPOL(NAPAR)
621         GO TO 902
622     906 CALL BLANK
623         WRITE(1,91)(ANPR(J),PARPOL(J),J=1,48)
624         GO TO 810
625   C
626   C   ## POS - PARAMETER OPTIMIZATION SEQUENCE ##
627   C
628     950 POS = .TRUE.
629         WRITE(1,69)
630         NAPAR = JEPARN(ANPR)
```

```
      WRITE(1,94)
      READ(1,71) NCON,PMIN,PMAX
      F = (PMAX-PMIN)/(FLOAT(NCON-1))
      D = PMIN
      DO 960 JZ = 1,NCON
      PARI(NAPAR) = D
      GO TO 501
  956 D = D + F
  960 CONTINUE
      WRITE(1,79)
      POS = .FALSE.
      GO TO 95
C
C   ## TE - TERMINATION OF PROGRAM
C
  990 JFITST = -12345
      TOK = .FALSE.
      PPTA = .FALSE.
      WRITE(5'1)(PARI(J),J=1,30),NPPE,(PLTMOD(J),J=1,6),(NGRTA(J),
     *J=1,4),(LINOPT(J),J=1,5),TITSIZ,XLSIZ,YLSIZ,(PLIMA(J),J=1,8),
     *(TIT(J),J=1,13),(XLAB(J),J=1,4),(YLAB(J),J=1,4)
      WRITE(5'2)((DRCTRY(J,K),J=1,5),K=1,30),(DRCSSG(J),J=1,30),FENTAV,
     *FENTUD,JFITST
      WRITE(1,99)
      STOP
      END
C
C
C                 &PLPAR WRITES OUT THE PLOT PARAMETERS
      SUBROUTINE &PLPAR(ANP,LINOPT,      TIT,XLAB,YLAB,PLS)
      LOGICAL PLTMOD(6)
      DIMENSION ANP(20),LINOPT(5),TIT(13),XLAB(4),YLAB(4),PLS(3),NUMP(6)
      COMMON/PLOTMU/PSAR(8),XSCF,YSCF,PLTMOD,NPLOVC,DUM(24),NGRTA(4),
     *SCRSIZ(4)
      DO 2 J = 1,6
      NUMP(J) = LGSW(PLTMOD(J),1,0)
    2 CONTINUE
      WRITE(1,10) ANP(1),(LINOPT(J),J=1,5),ANP(2),(NUMP(J),J=1,6),
     *(ANP(J+2),NGRTA(J),J=1,4),ANP(7),(TIT(J),J=1,13),ANP(8),PLS(1),
     *ANP(9),(XLAB(J),J=1,4),ANP(10),PLS(2),ANP(11),(YLAB(J),J=1,4),
     *ANP(12),PLS(3),(ANP(J+12),PSAR(J),J=1,8)
      RETURN
```

```
673      10 FORMAT(/A4,5X,5I1,9H LINOPTS /A4,4X,611,7H MODES /4(A4,8X,12/),
674        *A4,4X,13A4/A4,F10.2/2(A4,4X,4A4/A4,F10.2/),4(A4,F10.2/),
675        *4(A4,G10.3/) )
676         END
677   C
678   C  SEDCRY SEARCHES THE DIRECTORY FOR A NAME.
679         INTEGER FUNCTION SEDRCY (JUF8,DRCSSG,FENTUD,DRCTRY)
680         INTEGER SEDRCY,FENTUD,DRCSSG(30),DRCTRY(5,30)
681         DIMENSION JUF8(4)
682         N = FENTUD
683       1 DO 2 J = 1,4
684         IF(JUF8(J) .NE.DRCTRY(J,N))GO TO 4
685       2 CONTINUE
686   C                   FOUND IT
687         SEDRCY = N
688         RETURN
689       4 N = DRCSSG(N)
690         IF(N.GT.0) GO TO 1
691   C                   IF N=0 WE ARE AT END OF SEARCH STRING - COULDN'T FIND IT
692         SEDRCY = 0
693         RETURN
694         END
695   C
696   C  JEPARN LOCATES A PARAMETER NAME FROM THE NAME LIST.
697         FUNCTION JEPARN(ANPR)
698         DIMENSION ANPR(41)
699       2 ANME = 0.0
700         READ(1,5)ANME
701         JEPARN =LOPARN(ANME,ANPR)
702         IF(JEPARN.GE.0) RETURN
703         WRITE(1,10)
704         GO TO 2
705       5 FORMAT(A4)
706      10 FORMAT(10H ERR NAME  )
707         END
708   C
709   C  ETARA - EQUATE TWO ARRAYS
710         SUBROUTINE ETARA(ARN,ARO,N)
711         DIMENSION ARN(1),ARO(1)
712         DO 2 J = 1,N
713       2 ARN(J) = ARO(J)
714         RETURN
```

```
      END
C
C
C  COUV - CALCULATE OUTPUT VARIABLES
      SUBROUTINE COUV(AIO,SIO,AI2,Q3OFF,VS,DVDT,VTR)
      LOGICAL Q3OFF
      DIMENSION AIO(5),SIO(3)
      COMMON/PARICO/DUM1(5),ANTR,CS,DUM2(6),C1,DUM3(12),RC1,DUM4(19)
      AI2 = AIO(2)/ANTR
      VS  = AIO(4)/(CS*ANTR)
      DVDT = AIO(2)/(C1*ANTR)
      VTR = 0.0
      IF(Q3OFF) VTR = ABS(AIO(5)/(C1*ANTR)+AIO(2)*RC1/ANTR)
      RETURN
      END
C
C  AMXSET - ACCUMULATE ABSOLUTE MAXIMUM AND SET TIME
      SUBROUTINE AMXSET(A,N,T)
      COMMON/PARICO/PARI(30),PARO(16)
      AA = ABS(A)
      IF(AA.LE.PARO(N)) RETURN
      PARO(N) = AA
      IF(N.LE.6) PARO(N+10) = T
      RETURN
      END
C
C
C  DIOD: THIS MODELS THE TWO DIODES IN THE PRIMARY CIRCUIT
      FUNCTION DIOD(CALC,V,JTRNON,AI)
      IF(JTRNON.LT.2) GO TO 4
      IF(V*AI.LT.0.0) GO TO 2
      JTRNON = 1
      VDPON = V
    2 DIOD = CALC
      RETURN
    4 IF(VDPON*AI.GT.0.0) GO TO 2
      DIOD = 0.0
      RETURN
      END
C
C  Q3 : MODELS THE HIGH-VOLTAGE TRANSISTOR SWITCH WITH DIODE QUAD.
      FUNCTION Q3(ARG,OFF,AI2)
```

```
      LOGICAL OFF,PRVOFF
      COMMON/PARICO /DUM1(15),RWTX,DUM2(6),RWSCR,DUM3(21),WL1,WL2
      DATA PRVOFF/.TRUE./
      IF(.NOT.OFF.AND.PRVOFF) WL2 = WL2 + RWSCR*ABS(ARG)
      IF(.NOT.PRVOFF.AND.OFF) WL1 = WL1 + RWTX*ABS(AI2)
      PRVOFF = OFF
      Q3 = 0.0
      IF(OFF) Q3 = ARG
      RETURN
      END
C
C
C
      FUNCTION NULSW (A,LP,LM)
      NULSW = LP
      IF(A.LE.0.0) NULSW= LM
      RETURN
      END
C
      FUNCTION LOPARN(ANME,ANPARI)                                    2330
      DIMENSION ANPARI(47)                                            2340
      IF(ANME.NE.0)GO TO 2                                            2350
      LOPARN=0                                                        2360
      RETURN                                                          2370
 2    DO4K=1,48                                                       2380
      IF(ANME.EQ.ANPARI(K))GO TO 6                                    2390
 4    CONTINUE                                                        2400
      LOPARN=-1                                                       2410
      RETURN                                                          2420
 6    LOPARN=K                                                        2430
      RETURN                                                          2440
      END                                                             2450
C
C
C
C  * * * * * * * * G R A P H I C S  P A C K A G E * * * * * * * * * * *
C
      BLOCK DATA
      COMMON /PLOTMU/ DUM1(13),NPLDVC,DUM2(26),SCRSIZ(4)
      DATA NPLDVC/1/,SCRSIZ/7.25,5.5,14.0,10.0/
      END
C
```

```
C   TAXSCN - PERFORMS VARIOUS PLOTTING FEATURES FOR ONE AXIS, SCANS POINTS FOR
C        MAX,MIN VALUES,DETERMINES SCALE FACTORS, LOCATES AND DRAWS GRID LINES
C        AND TICS
C
      SUBROUTINE TAXSCN(NAX,NPTS,NT,TRCAR,JTR)
      LOGICAL PLTMOD(6)
      DIMENSION TRCAR(100,7),JTR(5)
      COMMON/PLOTMU/PMAR(4),AXEX(4),SCF(2)    ,PLTMOD,NPLOVC,AGP(12),
     *AGV(12),NGRTA(4),SCRSIZ(4)
      IF(.NOT.PLTMOD(NAX*3-2)) GO TO 20
      J = 1
      IF(NAX.EQ.2)J = NT
      AMIN = 1.0E9
      AMAX =-1.0E9
      DO 6 K = 1,NT
      M = 1
      IF(NAX.EQ.2) M = JTR(K) + 1
      DO 4 L = 1, NPTS
      IF(AMIN.GT.TRCAR(L,M)) AMIN = TRCAR(L,M)
      IF(AMAX.LT.TRCAR(L,M)) AMAX = TRCAR(L,M)
    4 CONTINUE
    6 CONTINUE
      IF(PLTMOD(NAX*3)) GO TO 10
C  FOR LINEAR PLOT EXTREMES ARE 10% OVER MAX AND UNDER MIN VALUES
      AXEX(2*NAX-1) = AMIN -0.1*(AMAX-AMIN)
      AXEX(2*NAX)   = AMAX +0.1*(AMAX-AMIN)
      GO TO 20
C     FOR LOG PLOTS EXTREMES ARE 10% OVER & UNDER LOG EXTREMES
   10 IF(AMIN.GT.0.0) GO TO 12
      WRITE(1,90)
      RETURN
   12 AL = ALOG10(AMAX/AMIN)
      AXEX(2*NAX-1) = AMIN*10.0**(-0.1*AL)
      AXEX(2*NAX)   = AMAX*10.0**(+0.1*AL)
C     DETERMINE SCALE FACTOR
   20 WIDE = SCRSIZ(NPLOVC*2+NAX-2)-PMAR(NAX*2-1)-PMAR(NAX*2)
      AMAX = AXEX(NAX*2)
      AMIN = AXEX(NAX*2-1)
      P1 = PMAR(5-NAX*2)
      P2 = P1 + 0.1
      P4 = SCRSIZ(NPLOVC*2-NAX+1)-PMAR(6-NAX*2)
      P3 = P4 - 0.1
```

```
      SLIM = SCRSIZ(NPLDVC*2+NAX-2)-PMAR(NAX*2)
      SCF(NAX) = WIDE/(AMAX-AMIN)
      IF(PLTMOD(NAX*3)) SCF(NAX) = WIDE/ALOG10(AMAX/AMIN)
      IF(PLTMOD(NAX*3-1)) GO TO 23
C     HERE FOR MANUAL GRID SPACING
      NGR = NGRTA(NAX)-2
      NTC = NGRTA(NAX+2)
      GSP = WIDE/FLOAT(NGR+1)
      TSP = GSP/FLOAT(NTC+1)
      GO TO 40
   23 IF(PLTMOD(NAX*3)) GO TO 30
C     HERE FOR AUTO GRID SPACING - LINEAR
   24 SIS = ALGCAT((AMAX-AMIN)/5.0)
      AGV(NAX*6-5) = SIS*FLOAT(JINT(AMIN/SIS) + 1)
      DO 28 J = 2,6
   28 AGV(NAX*6+J-6) = AGV(NAX*6-5) + FLOAT(J-1)*SIS
      GO TO 38
C     HERE FOR AUTO GRID SPACING - LOG
   30 AL = ALOG10(AMAX/AMIN)
      IF(AL.LT.0.9) GO TO 24
      IF(AL.LT.2.0) GO TO 34
      AGV(NAX*6-5) = 10.0**(JINT(ALOG10(AMIN)+1))
      DO 32 J = 1,5
   32 AGV(NAX*6+J-5) = AGV(NAX*6-5)*10.0**J
      GO TO 38
   34 AGV(NAX*6-5) = ALGCAT(AMIN)
      DO 36 J = 1,5
   36 AGV(NAX*6+J-5) =ALGCAT(   AMIN       *2.1545**J)
   38 DO 39 J = 1,6
   39 AGP(NAX*6+J-6) =AXMAP(NAX,AGV(NAX*6+J-6))
C     DRAW GRID LINES & TICS - MANUAL
   40 IF(PLTMOD(NAX*3-1)) GO TO 50
      DO 42 J = 1,NGR
   42 CALL DRLIN(NAX,PMAR(NAX*2-1)+GSP*FLOAT(J), P1 , P4,SLIM)
      NTC=(NGR+1)*(NTC+1)
      DO 44 J = 1, NTC
   44 CALL DRLIN(NAX,PMAR(NAX*2-1)+TSP*FLOAT(J),P1,P2,SLIM)
      DO 46 J = 1,NTC
   46 CALL DRLIN(NAX,PMAR(NAX*2-1)+TSP*FLOAT(J),P4,P3,SLIM)
      RETURN
C     DRAW GRID LINES AND TICS - AUTO
   50 DO 52 J = 1,6
```

```
      52 CALL DRLIN(NAX,AGP(NAX*6+J-6),P1,P4,SLIM)
         IF(PLTMOD(NAX*3)) GO TO 60
      54 TSP = SIS/5.0
         IF(ABS(FUNK(ALOG10(SIS)+10.0)-0.3).LT.0.1)TSP = SIS/4.0
         TVF= TSP*FLOAT(JINT(AMIN/TSP)+1)
         DO 56 J = 1,30
      56 CALL DRLIN(NAX,AXMAP(NAX,TVF+TSP*FLOAT(J-1)),P1,P2,SLIM)
         DO 58 J = 1,30
      58 CALL DRLIN(NAX,AXMAP(NAX,TVF+TSP*FLOAT(J-1)),P4,P3,SLIM)
         RETURN
      60 IF(AL.LT.0.9) GO TO 54
         IF(AL.LT.2.0) RETURN
         TVF = ALGCAT(AMIN)
         DO 62 J = 1,18
      62 CALL DRLIN(NAX,AXMAP(NAX,TVF*2.1545**J),P1,P2,SLIM)
         DO 64 J = 1,18
      64 CALL DRLIN(NAX,AXMAP(NAX,TVF*2.1545**J),P4,P3,SLIM)
         RETURN
      90 FORMAT(36H ERR NONPOSITIVE VALUES ON LOG PLOT)
         END
C
C
         SUBROUTINE DRLIN(NAX,TPOS,TSTRT,TEND,SLIM)
         IF(ABS(TPOS).GT.SLIM)RETURN
         CALL PEN(SW(NAX,TPOS,TSTRT),SW(NAX,TSTRT,TPOS),3)
         CALL PEN(SW(NAX,TPOS,TEND),SW(NAX,TEND,TPOS),2)
         RETURN
         END
C
C
         FUNCTION SW(NAX,X,Y)
         IF(NAX - 1) 2,2,4
       2 SW = X
         RETURN
       4 SW = Y
         RETURN
         END
C
C
C                PLOTA = DRAWS LINES ON PLOT, CALLED ONCE FOR EACH LINE DRAWN.
C              THIS VERSION ALSO PASSES OVER NONVALID POINTS IN PAR POOL MODE
CC
```

```
      SUBROUTINE PLOTA(NPTS,X,Y,LINOPT,PPTA,D)
      LOGICAL PPTA, VLDPT,AXOUT
      DIMENSION X(1),Y(1),D(1)
      VLDPT(L)= .NOT.PPTA .OR. LINOPT.EQ.D(L)
      PX = AXMAP(1,X(1))
      PY = AXMAP(2,Y(1))
      OPX = PX
      OPY = PY
      CALL DRAW (PX,OPX,PY,OPY,LINOPT,1)
      IF(VLDPT(1)) CALL DRAW(PX,OPX,PY,OPY,LINOPT,0)
      DO 10 J = 2,NPTS
      IF(.NOT.VLDPT(J)) GO TO 10
      PX = AXMAP(1,X(J))
      PY = AXMAP(2,Y(J))
      IF((AXOUT(PX,1).OR.AXOUT(PY,2)).AND.(AXOUT(OPX,1).OR.AXOUT(OPY,2))
     *) GO TO 9
      IF(.NOT.(AXOUT(OPX,1).OR.AXOUT(OPY,2)).AND.(AXOUT(PX,1).OR.
     *AXOUT(PY,2))) GO TO 6
      IF(.NOT.(AXOUT(PX,1).OR.AXOUT(PY,2)).AND.(AXOUT(OPX,1).OR.
     *AXOUT(OPY,2))) GO TO 8
C                HERE IF EVERYTHING IN BOUNDS
      CALL DRAW(PX,OPX,PY,OPY,LINOPT,0)
      GO TO 9
C                HERE IF POINT AWOL BUT PREVIOUS POINT IN
    6 CALL INTRP(PX,OPX,PY,OPY,PXN,PYN,0)
      CALL DRAW (PXN,OPX,PYN,OPY,LINOPT,0)
      GO TO 9
C                HERE IF POINT IN BUT PREVIOUS POINT AWOL
    8 CALL INTRP(PX,OPX,PY,OPY,PXN,PYN,1)
      CALL DRAW(PX,PXN,PY,PYN,LINOPT,0)
C                HERE IN ANY CASE
    9 OPX = PX
      OPY = PY
   10 CONTINUE
      RETURN
      END
C
C
C
      SUBROUTINE INTRP(PX,OPX,PY,OPY,PXN,PYN,NX)
      LOGICAL AXOUT
      COMMON /PLOTMU/ PMAR(4),DUM1(9),NPLOVC,DUM2(26),SCRSIZ(4)
```

```
      PINTX(GMAR) = OPX + (PX-OPX)*(GMAR-OPY)/(PY-OPY)
      PINTY(GMAR) = OPY + (PY-OPY)*(GMAR-OPX)/(PX-OPX)
      BMAR = PMAR(3)
      HIGH = SCRSIZ(NPLOVC*2) - PMAR(4)
      FMAR = PMAR(1)
      WIDE = SCRSIZ(NPLOVC*2-1) - PMAR(2)
      TX = PX
      TY = PY
      IF(NX.EQ.0) GO TO 2
      TX = OPX
      TY = OPY
    2 IF(.NOT.AXOUT(TX,1)) GO TO 4
    3 IF(TX-4.0) 12,12,10
    4 IF(TY - 3.0) 16,16,14
   10 PXN = WIDE
      PYN = PINTY(WIDE)
   11 IF(AXOUT(PYN,2)) GO TO 18
      RETURN
   12 PXN = FMAR
      PYN = PINTY(FMAR)
      GO TO 11
   14 PYN = HIGH
      PXN = PINTX(HIGH)
   15 IF(AXOUT(PXN,1)) GO TO 20
      RETURN
   16 PXN = PINTX(BMAR)
      PYN = BMAR
      GO TO 15
   18 TY = PYN
      GO TO 4
   20 TX = PXN
      GO TO 3
      END
C
C
      LOGICAL FUNCTION AXOUT(Z,L)
      LOGICAL AXOUT
      COMMON /PLOTMU/PMAR(4),DUM1(9),NPLOVC,DUM2(26),SCRSIZ(4)
      AXOUT = Z.LT.PMAR(2*L-1) .OR. Z.GT.(SCRSIZ(NPLOVC*2 + L-2) - PMAR(
     *2*L))
      RETURN
      END
```

```
C
C                DRAW: ENTERED ONCE FOR EACH POINT TO BE DRAWN.
C              LINOPTS: 1= CONTINUOUS; 2= DASHED(LONG); 3= DASHED(SHORT);
C              4,6,8: +,X,O MARKS RESPECTIVELY, WITH LINE DRAWN IN
C              BETWEEN POINTS; 5,7,9: LIKE 4,6,8 EXCEPT POINTS ONLY.
      SUBROUTINE DRAW(PX,OPX,PY,OPY,LINOPT,JI)
      IF(LINOPT.EQ.0) RETURN
      IF(JI.EQ.0) GO TO 2
      JFLG = 1
      RETURN
    2 IF(JFLG.EQ.0) GO TO 4
      OPX = PX
      OPY = PY
      JFLG = 0
      PEDO = 0.0
      GO TO 19
    4 PEDO = SQRT((PX-OPX)**2 + (PY-OPY)**2) + PEDO
      GO TO (10,20,30,10,50,10,70,10,90),LINOPT
   10 CALL PEN(OPX,OPY,3)
      CALL PEN(PX,PY,2)
   19 GO TO(99,99,99,50,50,70,70,90,90),LINOPT
   20 CALL PEN(OPX,OPY,3)
      DASH = .25
   21 RSEG = DASH*(1.0-FUNK(PEDO/DASH))
      IF(FUNK(PEDO*0.5/DASH).GT.0.5) GO TO 24
      IF(RSEG.GT.PED-PEDO) GO TO 10
      PIX = (PX-OPX)*RSEG/(PED-PEDO) + OPX
      PIY = (PY-OPY)*RSEG/(PED-PEDO) + OPY
      CALL PEN(PIX,PIY,2)
   22 OPX = PIX
      OPY = PIY
      PEDO = PEDO + RSEG + 0.003
      GO TO 21
   24 IF(RSEG.GT.PED-PEDO) GO TO 95
      PIX = (PX-OPX)*RSEG/(PED-PEDO) + OPX
      PIY = (PY-OPY)*RSEG/(PED-PEDO) + OPY
      CALL PEN(PIX,PIY,3)
      GO TO 22
   30 CALL PEN(OPX,OPY,3)
      DASH = .125
      GO TO 21
   50 CALL QUL(26,PX-0.02,PY-0.03,.06,0.0,OOPX,OOPY)
```

```
      GO TO 99
   70 CALL QUL(26,PX-0.02,PY-0.03,.06,.79,OOPX,OOPY)
      GO TO 99
   90 CALL QUL(48,PX-0.02,PY-0.03,.06,0.0,OOPX,OOPY)
      GO TO 99
   95 IF(((PY-OPY)*(OPY-OOPY).GE.0.0).AND.((PX-OPX)*(OPX-OOPX).GE.0.0))
     * GO TO 99
      PEDO = 0.0
      GO TO 4
   99 PEDO = PED
      OOPX = OPX
      OOPY = OPY
      RETURN
      END
C
C
C
C  ALGCAT - FIND DECADE POWER * 2,5 OR 10 NEXT GREATER THAN NUMBER
      FUNCTION ALGCAT(F)
      ADEC = 10.0**JINT(ALOG10(F))
      FLOG = FUNK(ALOG10(F) + 10.0)
      IF(FLOG.GT.0.699) ALGCAT = ADEC*10.0
      IF(FLOG.LE.0.699) ALGCAT = ADEC*5.0
      IF(FLOG.LE.0.301) ALGCAT = ADEC*2.0
      RETURN
      END
C
C  MAP A POINT - ONE AXIS
      FUNCTION AXMAP(NAX,PT)
      LOGICAL PLTMOD
      COMMON/PLOTMO/PMAR(4),AXEX(4),SCF(2),PLTMOD(6),JUM(61)
      PMIN = AXEX(NAX*2-1)
      IF(PLTMOD(NAX*3)) GO TO 4
      AXMAP = (PT-PMIN)*SCF(NAX) + PMAR(NAX*2-1)
      RETURN
    4 IF(PT.GT.0.0) GO TO 6
      WRITE(1,10)
    6 AXMAP = ALOG10(PT/PMIN)*SCF(NAX) + PMAR(NAX*2-1)
      RETURN
   10 FORMAT(36H ERR NONPOSITIVE VALUE ON LOG PLOT )
      END
C
```

```
      DOUBLE PRECISION FUNCTION CBIAS(E)
      DOUBLE PRECISION CBIAS,PCKUP
      COMMON /CBDROP/ PCKUP,LZ
      CALL CB(E)
      CBIAS = PCKUP
      RETURN
      END
C
      SUBROUTINE CB(E)
      LOGICAL SCNOT,PEXP,LFHF
      DIMENSION DEC(4),M(10)
      COMMON /CBDROP/L(3),JZF
      DATA DEC/1000.,100.,10.,1./,M(6)/46/
      CALL CLRBUF(L(1),3)
      M(1) = NULSW(-E,45,0)
      JZF = 0
      IF(E.EQ.0.0) GO TO 24
      F = ABS(E)
      IF(F.GE.0.00099) GO TO 4
      SCNOT = .TRUE.
      PEXP = .FALSE.
      NEXP = -INT(ALOG10(F) - 2.0)
      G = F*DEC(3)**NEXP + 0.5
      GO TO 10
    4 IF(F.LE.9999.0) GO TO 8
      SCNOT = .TRUE.
      PEXP = .TRUE.
      NEXP = INT(ALOG10(F) - 1.0)
      G = F/(DEC(3)**NEXP) + 0.5
      GO TO 10
    8 SCNOT = .FALSE.
      G = F
      IF(FUNK(G).NE.0.0) G = G + 0.00005
   10 M(2) = JZB(JINT(G/DEC(1)) + 48)
      DO 12 J = 3,5
   12 M(J) = JZB(MOD(JINT(G/DEC(J-1)),10) + 48)
      JZF = 0
      DO 14 J = 1,4
   14 M(11-J) = JZB(MOD(JINT(G*10.0*DEC(J)),10) + 48)
      LFHF = .TRUE.
      K = 1
      DO 20 J = 1,10
```

```
      IF(SCNOT .AND. J.GE.6) GO TO 16
      IF(M(J).EQ.0) GO TO 20
      IF(J.EQ.6 .AND. FUNK(G).EQ.0.0) RETURN
      GO TO 18
   16 IF(J.EQ.6) GO TO 18
      IF(J.EQ.7) M(7) = LGSW(PEXP,43,45)
      IF(J.EQ.8) M(8) = NEXP + 48
      IF(J.EQ.9) RETURN
   18 L(K) = LGSW(LFHF,M(J)*256+32,L(K)-32+M(J))
      LFHF = .NOT. LFHF
      IF(LFHF) K = K + 1
      IF(K.GE.4) RETURN
   20 CONTINUE
      RETURN
   24 L(1) = 8240
      RETURN
      END
C
      FUNCTION JZB(MARG)
      COMMON /LBDROP/L(3),JZF
      JZB = 0
      IF(JZF.EQ.1 .OR. MARG.NE.48) GO TO 3
      RETURN
    3 JZB = MARG
      JZF = 1
      RETURN
      END
C
      FUNCTION JINT(G)
      IF(ABS(G).GT.9999.0) GO TO 2
      JINT = INT(G)
      IF(G.LT.0.0) JINT = JINT - 1
      RETURN
    2 JINT = 0
      RETURN
      END
C
      FUNCTION FUNK(X)
      FUNK = X - AINT(X)
      RETURN
      END
C
```

```
C
      SUBROUTINE CLRBUF(JUF,N)
      DIMENSION JUF(1)
      DATA JBLK/2H  /
      DO 2 J = 1,N
    2 JUF(J) = JBLK
      RETURN
      END
C
C
      SUBROUTINE BOUL(JUFR,NCC,PX,PY,CHT,ANG)
      DIMENSION JUFR(2)
      DATA DSX,DSY/2*0.0/
      SX = PX
      SY = PY
      DO 3 J = 1,NCC
      NC = IAND(JUFR(J/2 + 1 ),4Z7F00)/256 - 32
      IF(MOD(J,2).EQ.0) NC = IAND(JUFR(J/2),4Z007F) - 32
      CALL QUL(NC,SX,SY,CHT,ANG,DSX,DSY)
      SX = SX + DSX
      SY = SY + DSY
    3 CONTINUE
      RETURN
      END
C
C
      SUBROUTINE QUL(NC,SX,SY,CHT,ANG,DSX,DSY)
      LOGICAL LHF
      INTEGER DRCTRY(64),STRX(320),SK1(80),SK2(80),SK3(80),SK4(80)
      EQUIVALENCE (STRX(1),SK1(1)),(STRX(81),SK2(1)),(STRX(161),SK3(1)),
     *(STRX(241),SK4(1))
      DATA DRCTRY/   0,   1,   5,   8,  14,  23,  37,  48,  50,  54,
     *              59,  65,  68,  70,  72,  74,  79,  86,  89,  94,
     *             101, 105, 111, 118, 121, 131, 138, 142, 144, 149,
     *             153, 157, 165, 180, 185, 194, 199, 205, 209, 213,
     *             220, 225, 230, 235, 240, 242, 245, 248, 256, 261,
     *             271, 277, 283, 286, 291, 293, 297, 300, 304, 307,
     *             310, 312, 316, 320/
      DATA SK1/4Z0180,4Z1411,4Z3120,4Z1102,4Z233F,4Z121D,4Z1902,4Z5D59,
     *         4Z1220,4Z4F12,4Z90BF,4Z1204,4ZE402,4Z1BFB,4Z1250,4Z6F12,
     *         4Z90AF,4Z0A22,4Z82C4,4ZC688,4Z583A,4Z3B6D,4Z6000,4Z1F5D,
     *         4Z4E3E,4Z1C1B,4Z2A3A,4Z5C5D,4Z8DBE,4Z5172,4Z9394,4Z1994,
```

```
      *          4ZB6C6,4ZE5E4,4ZB2A2,4Z9394,4Z01E4,4Z16A4,4Z5525,4Z2769,
      *          4Z8915,4Z695A,4Z5B9D,4ZCD12,4Z9DAF,4Z1263,4Z5001,4ZC000,
      *          4Z0328,4Z3B3D,4Z0630,4Z1206,4Z081D,4Z3F00,4Z1600,4Z2236,
      *          4Z382D,4Z0F01,4Z4000,4Z1282,4Z8D12,4Z44CC,4Z124C,4ZC402,
      *          4Z28E6,4Z1280,4Z8F02,4Z08F8,4Z0300,4Z2325,4Z0208,4ZF800,
      *          4Z0213,4Z1100,4Z02C0,4ZAF00,4Z0000,4Z0000,4Z0000,4Z0D9A/
       DATA SK2/4Z9973,4Z5222,4Z1305,4Z185C,4Z4D7D,4Z8C9A,4Z1322,4Z3D2B,
      *          4Z014B,4Z082C,4Z5D6D,4Z8C8A,4Z7702,4Z9200,4Z1A2D,4Z9D26,
      *          4Z5776,4Z8472,4Z5020,4Z0101,4Z9000,4Z127D,4Z5003,4Z6D03,
      *          4ZA300,4Z0A01,4Z2050,4Z8294,4Z8657,4Z162D,4Z8D00,4Z0C17,
      *          4Z395A,4Z7987,4Z7452,4Z3213,4Z0518,4Z8F00,4Z131D,4ZAD00,
      *          4Z01A0,4Z1F8D,4ZAB27,4Z1615,4Z2352,4Z6293,4Z9688,4Z4A3B,
      *          4Z3E5F,4Z035F,4Z9FBD,4Z1B66,4Z4535,4Z1608,4Z2C5D,4Z7C8A,
      *          4Z6610,4Z0190,4Z1208,4ZF812,4Z707F,4Z01F0,4Z0208,4ZF800,
      *          4Z1600,4Z2236,4Z392D,4Z0F01,4Z4F00,4Z1203,4Z0512,4Z0A0C,
      *          4Z011C,4Z1411,4Z3120,4Z1102,4Z233F,4Z1421,4Z4130,4Z2118/
       DATA SK3/4Z3346,4Z689B,4Z9D7F,4Z3F1E,4Z01AE,4Z1F87,4Z7656,4Z4746,
      *          4Z5A7B,4Z9B87,4Z8695,4ZB5D6,4ZF9FA,4Z1BFA,4ZEDBF,4Z7F2E,
      *          4Z0A05,4Z2150,4Z90E1,4Z01F1,4Z1302,4Z6FA1,4Z1214,4Z9301,
      *          4ZB300,4Z1802,4Z1D6D,4Z9C99,4Z7756,4Z1616,4Z5675,4Z8483,
      *          4Z6202,4Z01A0,4Z0873,4Z5212,4Z051B,4Z3D6D,4Z8C00,4Z1902,
      *          4Z1D4D,4Z7C88,4Z8674,4Z3202,4Z0190,4Z1217,4Z6704,4Z8202,
      *          4Z1D9D,4Z1217,4Z6703,4Z011D,4Z9D00,4Z199C,4Z7D3D,4Z1B04,
      *          4Z1130,4Z5185,4Z0335,4ZA5A3,4Z1202,4Z1D12,4Z92AD,4Z0207,
      *          4ZA700,4Z1200,4Z2012,4Z102F,4Z021F,4Z3F00,4Z1502,4Z2030,
      *          4Z627D,4Z021D,4ZCD00,4Z1202,4Z1D12,4Z059E,4Z0238,4Z9000/
       DATA SK4/4Z031D,4Z0191,4Z0501,4Z4E76,4ZFEE1,4Z0401,4Z1E71,4Z8E00,
      *          4Z0FB7,4ZA493,4Z6242,4Z1306,4Z081B,4Z2C5D,4Z7DAC,4ZB9B7,
      *          4Z1701,4Z1D5D,4Z8C89,4Z6515,4Z0195,4Z1FB7,4ZA493,4Z6242,
      *          4Z1306,4Z081B,4Z2C5D,4Z7DAC,4ZB9B7,4Z0295,4ZD000,4Z1701,
      *          4Z1D5D,4Z8C89,4Z6515,4Z0365,4Z8190,4Z0B02,4Z7293,4ZA587,
      *          4Z4728,4Z1A2C,4Z4DBD,4Z1250,4Z6E02,4Z0ECE,4Z081D,4Z0513,
      *          4Z3242,4Z7395,4ZAD00,4Z050E,4Z41BE,4Z130F,4Z41AD,4Z036D,
      *          4Z91FF,4Z121E,4Z8202,4Z00BE,4Z1331,4Z491E,4Z0249,4ZAF00,
      *          4Z041D,4Z8D02,4Z8200,4Z0456,4Z000F,4Z5F00,4Z020F,4ZF000,
      *          4Z1400,4Z505F,4Z0F01,4Z6F00,4Z1240,4Z4F03,4Z064F,4Z8800/
       ICHR = DRCTRY(NC+1)
       CHT16 = CHT/ 16.0
       CANG = COS(ANG)
       SANG = SIN(ANG)
       LHF = .FALSE.
     4 JSTRK = KSTRK(STRX,ICHR,LHF)
```

```
      MORE = IAND(JSTRK,4Z00F0)
      NSTRK = IAND(JSTRK,4Z000F)
      JPEN = 3
    5 DO 8 J = 1,NSTRK
      JSTRK = KSTRK(STRX,ICHR,LHF)
      JX = IAND(JSTRK,4Z00F0)/16
      JY = IAND(JSTRK,4Z000F)
      DSX = CHT16*(FLOAT(JX)*CANG - FLOAT(JY)*SANG)
      DSY = CHT16*(FLOAT(JY)*CANG + FLOAT(JX)*SANG)
      CALL PEN(SX+DSX,SY+DSY,JPEN)
      JPEN = 2
    8 CONTINUE
      IF(MORE.NE.0) GO TO 4
      DSX = CHT16*CANG*FLOAT(JX+3)
      DSY = CHT16*SANG*FLOAT(JX+3)
      RETURN
      END
C
C
      FUNCTION KSTRK(STRX,ICHR,LHF)
      INTEGER STRX(500)
      LOGICAL LHF
      LHF = .NOT.LHF
      IF(LHF) ICHR = ICHR + 1
      KSTRK = LGSW(LHF,ISHFT(STRX(ICHR),-8),STRX(ICHR))
      RETURN
      END
C
      FUNCTION LGSW(L,JT,JF)
      LOGICAL L
      LGSW = JF
      IF(L) LGSW = JT
      RETURN
      END
C
C
      SUBROUTINE PEN(X,Y,JPEN)
      LOGICAL PENDWN
      COMMON/PLOTMU/DUM1(13),NPD,DUM2(30)
      DATA JPAGE,FA/850,100./,JARK/4Z021D/
      IF(JPEN.EQ.20) GO TO 10
      IF(JPEN.GE.8) GO TO 40
```

```
      IF(JPEN.GE. 1) GO TO 20
      IF(JPEN.EQ.-3) GO TO 5
C         INITIALIZATION/TERMINATION PROCEDURES. HERE FOR JPEN = 0
      GO TO (1,3),NPD
    1 CALL DRVR(-2)
      GO TO 10
    3 CALL DRVR(17)
      CALL MOVER(JOX,0,JRX,0)
      GO TO 6
    5 CALL DRVR(-1)
      IF(NPD.EQ.2) GO TO 6
      CALL BLANK
      GO TO 10
    6 CALL DRVR(17)
      CALL MOVER(0,0,0,-1200)
      CALL MOVER(0,0,0,50)
      CALL DRVR(-2)
   10 JOX = 0
      JOY = 0
      JRX = 850
      PENDWN = .FALSE.
      RETURN
C             NORMAL ENTRY
   20 IF(JPEN.NE.2) GO TO 22
      PENDWN = .TRUE.
      IF(NPD.EQ.2) CALL DRVR(0)
   22 IF(JPEN.NE.3) GO TO 23
      PENDWN = .FALSE.
      IF(NPD.EQ.2) CALL DRVR(17)
   23 GO TO (24,26),NPD
   24 JNX = ITEK(X,64)
      JNY = ITEK(Y,96)
      GO TO 28
   26 JNY = IFUNC(Y)
      JNX = IFUNC(X)
   27 IF(JNX.LT.JRX) GO TO 28
      JRX = JRX + JPAGE
      GO TO 27
   28 IF(JOX.EQ.JNX.AND.JOY.EQ.JNY) RETURN
      GO TO (29,31), NPD
   29 IF(.NOT.PENDWN) CALL DRVR(JARK)
      CALL DRVR(JNY)
```

```
      CALL DRVR (JNX)
   30 JOX = JNX
      JOY = JNY
      RETURN
   31 CALL MOVER (JOX,JOY,JNX,JNY)
      GO TO 30
C             PEN LIFT/DROP ENTRIES
   40 CALL DRVR (-2)
      IF (JPEN.NE.8) GO TO 42
      PENDWN = .TRUE.
      IF (NPD.EQ.2) CALL DRVR (0)
   42 IF (JPEN.NE.9) RETURN
      PENDWN = .FALSE.
      IF (NPD.EQ.2) CALL DRVR (17)
      RETURN
      END
C         DRVR IS ENTERED ONCE FOR EACH WORD OUTPUTTED TO DEVICES.
      SUBROUTINE DRVR (IARG)
      DIMENSION ITAB (18),IBUF (121),IUFT (6)
      COMMON /PLOTMU/DUM1(13),NPD,DUM2(30)
      DATA ITAB/32,1,9,8,9,8,10,2,10,2,6,4,6,4,5,1,5,16/,
     *IUFT/ 0,4ZAF00,4*0/
      IF(IARG + 1) 86,10,20
   10 DO 15 I = 1,121
   15 IBUF(I) = 0
      I = 1
      RETURN
   20 IBUF(I) = IARG
      IF(NPD.EQ.2) IBUF(I) = ITAB(IARG + 1)
      I = I + 1
      IF(I.LT.33) RETURN
      IF(NPD.EQ.2.AND.I.LT.121) RETURN
   86 IF (NPD.EQ.1) CALL WRITE(IBUF,(I-1)*2,IUFT,.TRUE.)
      IF(NPD.EQ.2) CALL PLT(IBUF(1))
      GO TO 10
      END
C
      SUBROUTINE BLANK
      WRITE(1,5)
    5 FORMAT(2HEL)
      DO 2 J = 1,32000
    2 K = J*7 + J/67
```

```
      RETURN
      END
C
      FUNCTION IFUNC(ARG)
      DATA FA/100./
      IFUNC = INT(ARG*FA)
      IF(IFUNC.LT.0) IFUNC = 0
      RETURN
      END
C
C
      FUNCTION ITEK(P,M)
      DATA RSTR/.00705/
      ITEK = (32+INT(P/RSTR)/32)*256 + M + MOD(INT(P/RSTR),32)
      IF(P.LT.0) ITEK = 8192 + M
      RETURN
      END
C
C
      SUBROUTINE MOVER(IXZ,IYZ,IXN,IYN)                                  MOVER.2
C * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * MOVER.3
C                                                                       *MOVER.4
C                                                                       *MOVER.5
C * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * MOVER.6
C     MOVER COMPUTES THE OPTIMUM PATH FOR MOVEMENT BETWEEN TWO POINTS. *MOVER.7
C     ENTRY* CALL MOVER(IXZ,IYZ,IXN,IYN)                                *MOVER.8
C     USAGE*                                                            *MOVER.9
C      (1) (IXZ,IYZ) ARE THE COORDINATES OF THE STARTING POINT.         *MOVER.10
C      (2) (IXN,IYN) ARE THE COORDINATES OF THE END POINT.              *MOVER.11
C     RESTRICTIONS*                                                     *MOVER.12
C      (1) MOVER REQUIRES THE SUPPORT ROUTINE DRVR.                     *MOVER.13
C                                                                       *MOVER.14
C * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * MOVER.15
      IA=IYN-IXZ                                                         MOVER.16
      IB=IYN-IYZ                                                         MOVER.17
      IF(IA)2,1,2                                                        MOVER.18
    1 IF(IB)2,21,2                                                       MOVER.19
   21 RETURN                                                             MOVER.20
    2 ID=IA+IB                                                           MOVER.21
      IT=IB-IA                                                           MOVER.22
      JA=IA
      JB=IB
```

```
      JD=ID
      JT=IT
      IF(JD.EQ.0)JD=1
      IF(JA.EQ.0)JA=1
      IF(JB.EQ.0)JB=1
      IF(JT.EQ.0)JT=1
      I=9+ISIGN (1,JB)+ISIGN (1,JD)+ISIGN (1,JT)                    MOVER.23
      I=9-ISIGN (I,JA)                                              MOVER.25
      IA=IABS(IA)                                                   MOVER.26
      IB=IABS(IB)                                                   MOVER.28
      IT=IA+IB                                                      MOVER.29
      ID=IB-IA                                                      MOVER.30
      IF(ID)13,12,12                                                MOVER.31
   12 IB=IA                                                         MOVER.32
      ID=-ID                                                        MOVER.33
   13 I1=I-1                                                        MOVER.34
      IA=IB+ID                                                      MOVER.35
      IB=IB+IB                                                      MOVER.36
      ID=ID+ID                                                      MOVER.37
   15 IF(IA)17,16,16                                                MOVER.38
   16 IA=IA+ID                                                      MOVER.39
       CALL DRVR(I)                                                MOVER.40
      IT = IT-2                                                     MOVER.41
      GO TO 18                                                      MOVER.42
   17 IA=IA+IB                                                      MOVER.43
      IT=IT-1                                                       MOVER.44
      CALL DRVR(I1)                                                 MOVER.45
   18 IF(IT)21,21,15                                                MOVER.46
      END                                                           MOVER.47
TOTAL RECORDS WRITTEN =   161
.EXIT
$EOJ  13:41:58
```

# APPENDIX B

# HEAT TRANSFER, STRESS ANALYSIS DESIGN

## B-1 COOLING AND HEAT TRANSFER

The power components in the system are mounted upon an aluminum channel that is cooled by a water line. The major power components include switching transistors, transformers, and resistors. The cooling system is designed to carry away a total of 8 kW of power with a maximum temperature rise of 30°F and a maximum pressure drop of 25 psi. The heat transfer from the inductor and the driver transistors is taken as representative of the worst case for heat-transfer efficiency.

The cooling system consists of eight 5-foot lengths of 1/8-inch i.d. copper tubing paralleled between two 1/4-inch i.d. manifolds. Each small copper tube cools one PWB board which dissipates a worst-case power of 1000 watts.

The inductor is mounted directly above the cooling tube. This inductor is approximately 1.5 inches in diameter, and approximately 0.04 inch of aluminum separates it from the nearest portion of the cooling tube. Because the tube is buried less than halfway into the aluminum, the effective width of the tube is only 0.1 inch as far as heat transfer is concerned. The effective heat-transfer area for this case is then 2.0 inches x 0.1 inch or 0.2 square inch.

Since approximately 0.4 inch of aluminum separates the nearest part of the tube from the inductor, and since the aluminum is 0.093 inch thick, an average heat-transfer length of 0.06 inch is not unreasonable.

The coefficient of conductivity for aluminum is 2.32 watt/inch-$^{o}$F. If we assume a joint coupling efficiency of 0.80, then the heat-transfer rate is 6.19 watt/$^{o}$F, far more than adequate.

Likewise, the transformer is mounted directly above a cooling tube. The transformer dissipates about double the heat of the inductor.

The driver transistors are mounted so that their centers are 0.5 inch away from the center of the water line. Both transistors together make a heat source approximately 2 inches long. This heat must be carried to the water line by the aluminum channel that is 0.093 inch thick. Hence the effective heat-transfer area is 0.186 square inch and the effective length is 0.5 inch. This gives a total heat-transfer rate for both transistors of 0.69 watt/$^{o}$F. This rate is an order of magnitude down from the previous case, but still adequate.

Consider a single 1/8-inch i.d. tube; it has an interval cross-sectional area of $8.522 \times 10^{-5}$ ft$^{2}$, and it must transfer 1000 watts of heat for a length of 5 feet, raising the internal water temperature no more than 30$^{o}$F. The required flow rate to remove this heat is $5.08 \times 10^{-4}$ ft$^{3}$/sec, or 0.227 gal/min. Since we have eight tubes in parallel, each with a maximum flow rate of 0.227 gal/min, the flow rate for the whole system is eight times that, or 1.82 gal/min. To get 0.227 gal/min through a 1/8-inch tube, the water must go through the tube at 5.94 ft/sec.

We can see that the rate of pressure drop across a single 1/8-inch i.d. tube with an interval flow of 0.227 gal/min is 200 feet of water per hundred feet of tube. For 5 feet of tube, this amounts to 4.33 psi. Since the tubes are in parallel, the pressure drop across all of them is the same as that across a single tube--4.33 psi.

These tubes are attached to two ½-inch i.d. manifolds 14 inches long. These manifolds are in series with each other and the whole system, so each one must carry the whole flow of 1.82 gal/min. The rate of head loss for such a tube and such a flow rate is about 250 feet of water per 100 feet of tube. For a total of 28 inches of tube, we get a pressure drop of 2.53 psi. When this figure is added to the pressure drop across the 1/8-inch tubes, we get a pressure drop across the whole system of 6.85 psi, well below the design ceiling of 25 psi.

## B-2 STRESS ANALYSIS

The container for the Linear Actuator Amplifier System has been analyzed for structural adequacy to withstand the vibrational and shock loading specified in the Airborne Laser Laboratory Reference Manual (ALLRM).

For purposes of this document, the following parameters have been adopted: for aluminum alloys an ultimate strength of 42,000 psi, a yield strength of 35,000 psi, and shear strength of 18,000 psi; for normal operating conditions, the design will limit stresses in structural members to 20,000 psi in tension and 8,000 psi in shear; for crash conditions, the design will limit stress level to 35,000 psi in tension and 12,000 psi in shear; the G-10 fiberglass panel used for the printed circuit board has a tensile strength of 25,000 psi; for normal operating conditions, design stresses within this material will be limited to 10,000 psi.

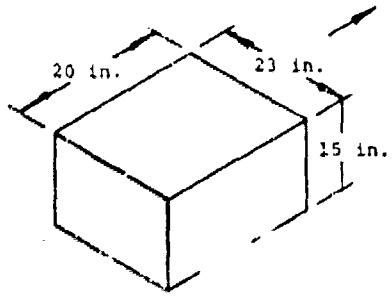
## B-3 INERTIAL LOADINGS

The inertial load factors to which the package may be subjected are as shown in Table 1 of the ALLRM, page 7. These

inertial load factors will be used to analyze the package in a non-rack mounted situation. Flight, taxi, takeoff, and landing loads act in combination; that is, the analysis must consider the simultaneous application of any combination of these load factors. The crash load factors, however, act separately upon the package. These load factors will not be used in life cycle predictions because they can only occur under unusual combinations of maneuvers. The structural design anticipates mounting the package with a four-point anchor bolt attachment. Figure B-1 shows computed tensile and shear loads acting on these bolts for the conditions shown. Stress analysis of critical components of the package indicate the stresses shown in Figure B-1. All of these stress levels are within the maximum indicated above.

## B-4 VIBRATION LOADINGS

The package will be analyzed to the load factor and amplifications shown in Figure B-2. This curve represents the sinusoidal amplitude input by base motion of the test specimen at the resonant frequency of the specimen for the ALL aircraft. Due to the compactness of the PWB board spacing, a 1 g sinusoidal input must be considered to ensure that no board touches another during normal operation. An analysis which considers the combined rigidity of the G-10 circuit board and of the aluminum channel that serves as a heat sink indicated a composite material rigidity of $3.15 \times 10^5$ psi-in$^4$. For purposes of determining the natural frequency of the printed circuit board, the following assumptions were made: that the printed circuit board is simply supported along the two shorter edges and is free along both of the longer edges; and that the weight of components is uniformly distributed over the surface. The components in question amount to approximately 11 pounds on each circuit board. The combination of




Four-point Non-rack Mounting

ANCHOR BOLT LOAD

| | Normal Operating | | Crash |
|---|---|---|---|
| Bolt Load | Flight (F-D-L) | Taxi, Take-off and Landing (F-L) | FWD |
| Max. Tension | 76.2 lb | | 500.0 lb |
| Max. Shear | | 50.2 lb | 720 lb |

FRAME STRESS LEVEL

| | Normal | | Crash |
|---|---|---|---|
| | Flight (down) | Taxi (Lateral) | FWD |
| 1-1/2 x 1-1/2 x 3/16 L | 5880 psi (Bending) | | 18720 psi (Bending) |
| Panel | | 45 psi Shear | 570 psi (Shear) |
| FWB Board | | 1590 psi (Bending) | |

Figure B-1. Loadings on anchor bolts and maximum stresses in structural members.

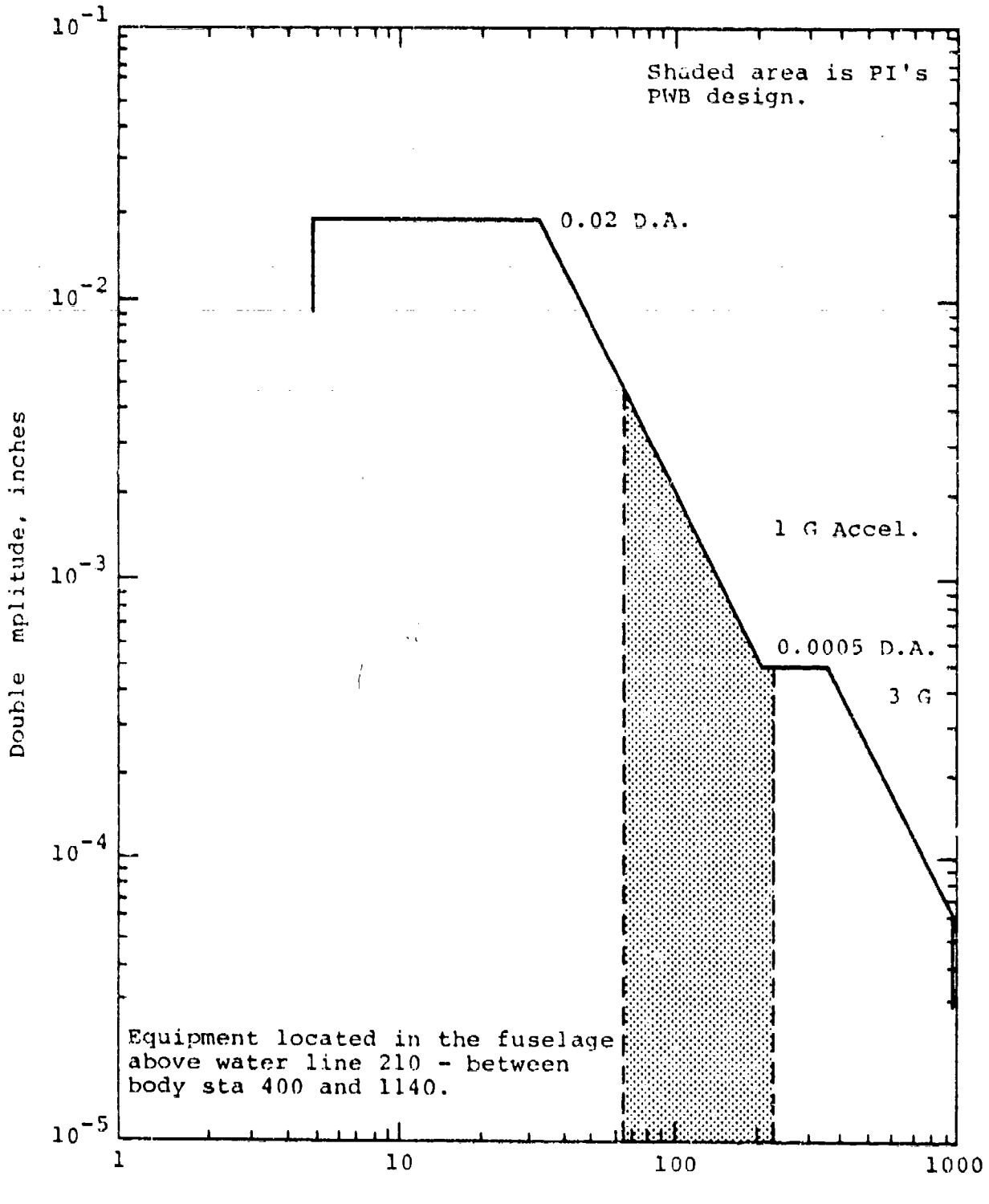



Figure B-2. Vibrational input system.

rigidity and mass loading indicated a natural frequency of the board of about 66 Hz. Figure B-2 indicates that the board will be subjected to 1 g dynamic loading at this frequency, so the total possible g loading will consist of the sum of the dynamic and inertial loadings or a total of 3.5 g. Further analysis indicates that the 1-g sinusoidal vibration input will excite a double amplitude of 0.07 inch in a printed circuit board. This selection is well within the tolerable maximum permitted by the board spacing incorporated into the design.

# APPENDIX C

# SUBSYSTEM HAZARD ANALYSIS

The actuator amplifier system has a single energy source, the 120 to 208 V, 400 Hz aircraft power supply. A single power connector brings it to the chassis, and a single circuit breaker disconnects it.

The system chassis is designed to remain physically intact in the event of an aircraft crash as described above.

The actuator output can rise in voltage to 1.5 kV across the actuators and above ground. One side of the actuator will always be within a few volts of ground. If input power fails or is shut off, if the cabinet cover on the high-voltage side is lifted, or if the flow of cooling water fails, the hot sides of all actuators are grounded and the power-on-reset circuitry prevents any additional high voltage from being generated. Any internal capacitors in the system not crowbarred at this point can carry only low voltage (110 V or less).

The system power supply is designed so that when it is started, the 112-V supply is the last to come up to voltage. This design eliminates any possibility of runaway conditions, e.g., a PS transistor turned on continuously on startup. Likewise, when the power supply is shut down or cut off, the 112-V supply is the first to go down. This feature will ensure that the preset input to the HVG flip-flop, which is connected to the 112-V supply through a divider, goes active-low while the logic is still functioning. As a result, the HVGs will be held on and allow the load to discharge; this can be done without danger of damaging components. The discharge would take 2 to 5 ms, and the +7-V supply will stay powered up at least that long.

The solid aluminum housing of the chassis provides protection against RFI/EMI. The cable carrying the 61 analog command inputs consists of 61 shielded cables, and the shields are internally connected to ground.

The screwdriver-adjusted trimpots are mounted in such a way that it is not possible to touch high voltage by inserting a screwdriver through any of the access holes to the trimpots.

# APPENDIX D

# SCHEMATIC DIAGRAMS

The overall schematic diagram submitted with the Phase I report was redrawn into four schematic diagrams at the time detailed artwork was done. These four pertained to the three PC boards: logic, "piggy back," and main/driver, and to the heat sink/power stage components. Each was the detailed schematic of one of the four major subassemblies of the prototype. These drawings were in the form of engineering sketches.

During the assembly and debugging effort these drawings were kept up-to-date with all changes made. Thus, they emerged in the form of "as-built" drawings. They are included here as Figures D-2 through D-5.

The common logic breadboard, built from that section of the overall schematic, was also kept up-to-date during the debugging effort, and is redrawn as an illustration; this is Figure 9.

A diagram of the overall setup of the prototype subassemblies, the common logic breadboard, and the power supplies was first submitted as an engineering drawing with the Equipment Test Plan. It is included here, as-built, in the form of an overall schematic illustrating the interrelationship of the subassemblies; this is Figure D-1.

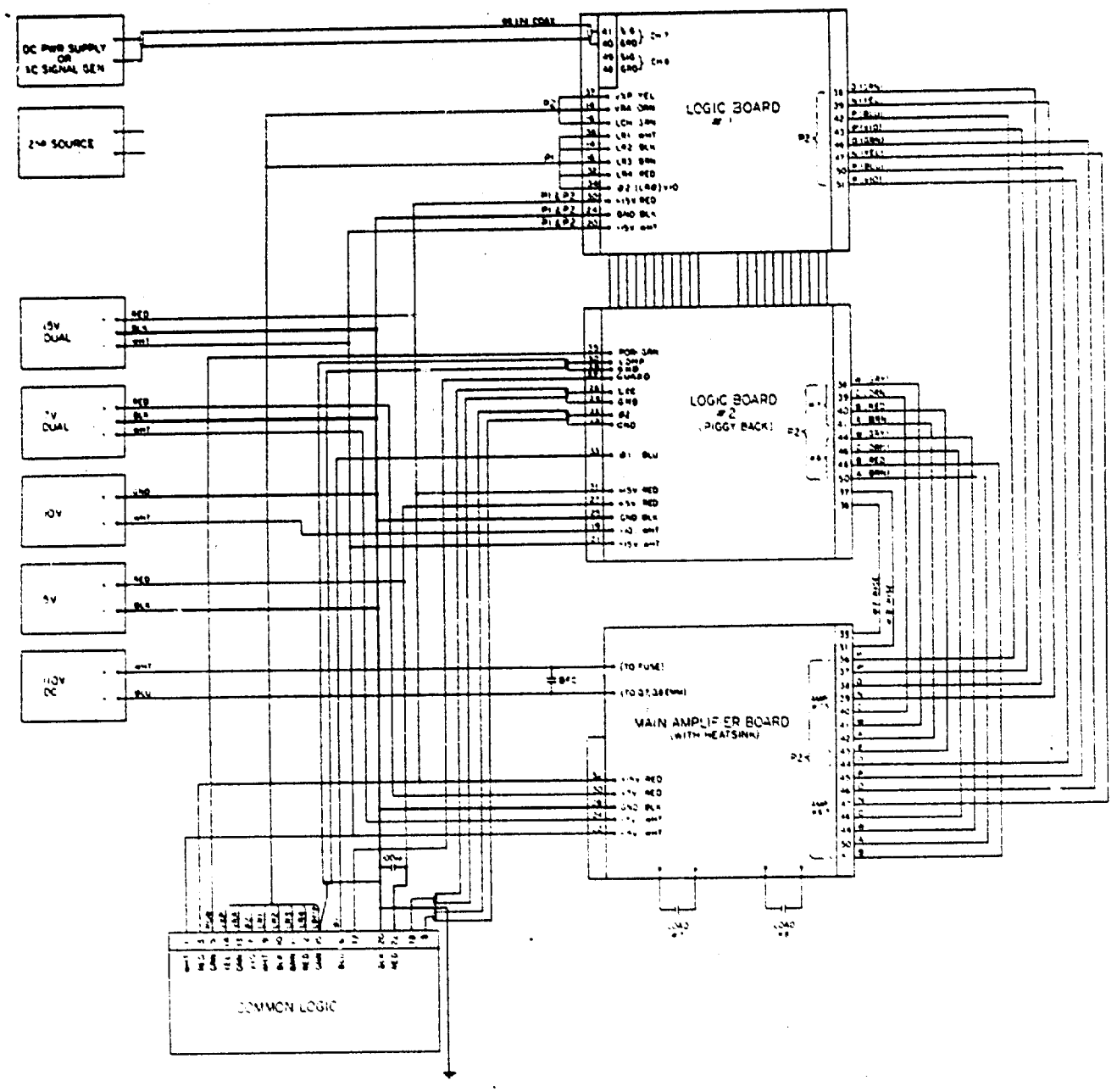



Figure D-1. Actuator amplifier prototype and common logic breadboard wiring diagram.

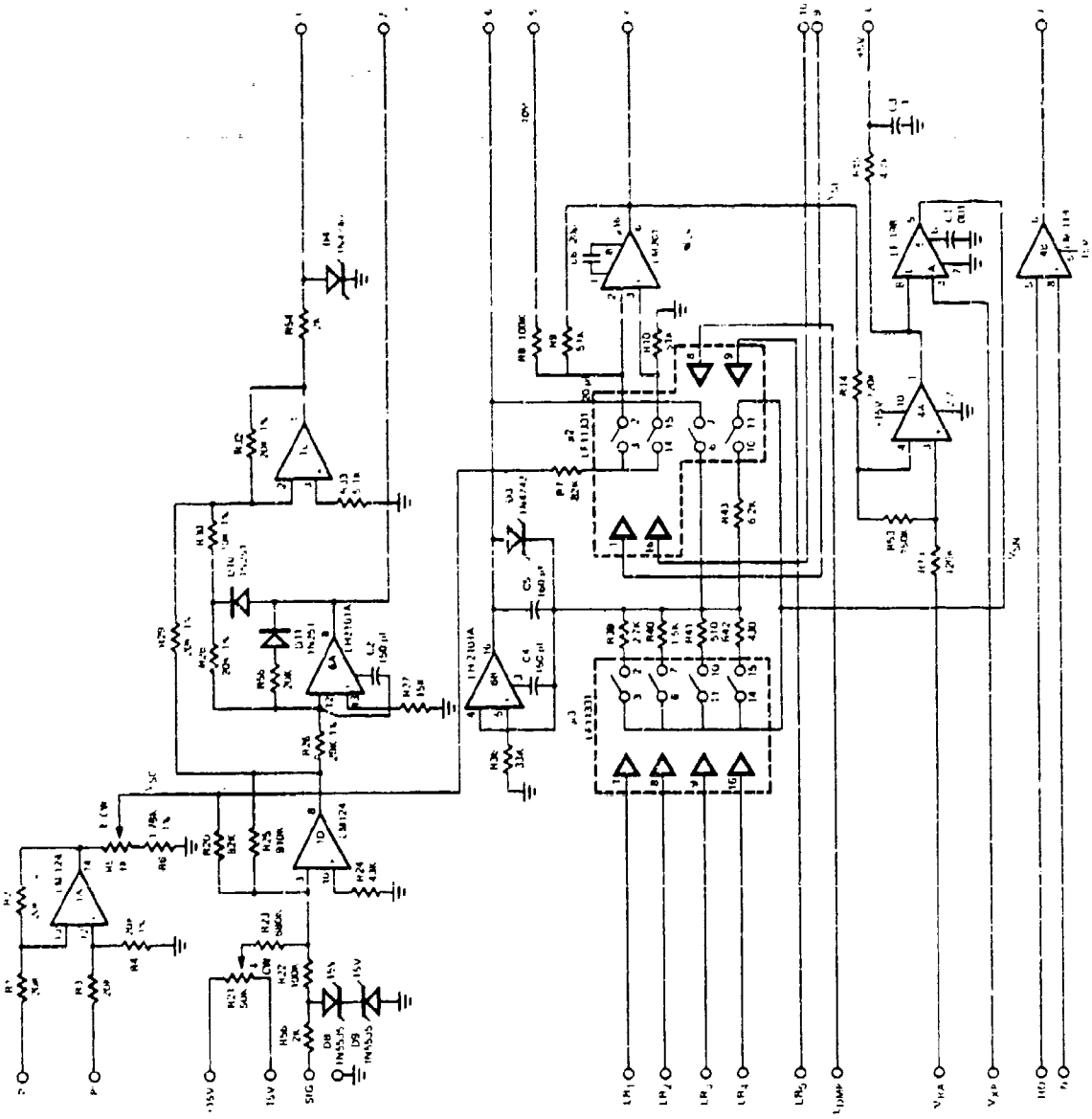


Figure D-2. Logic PC board No. 1 schematic.

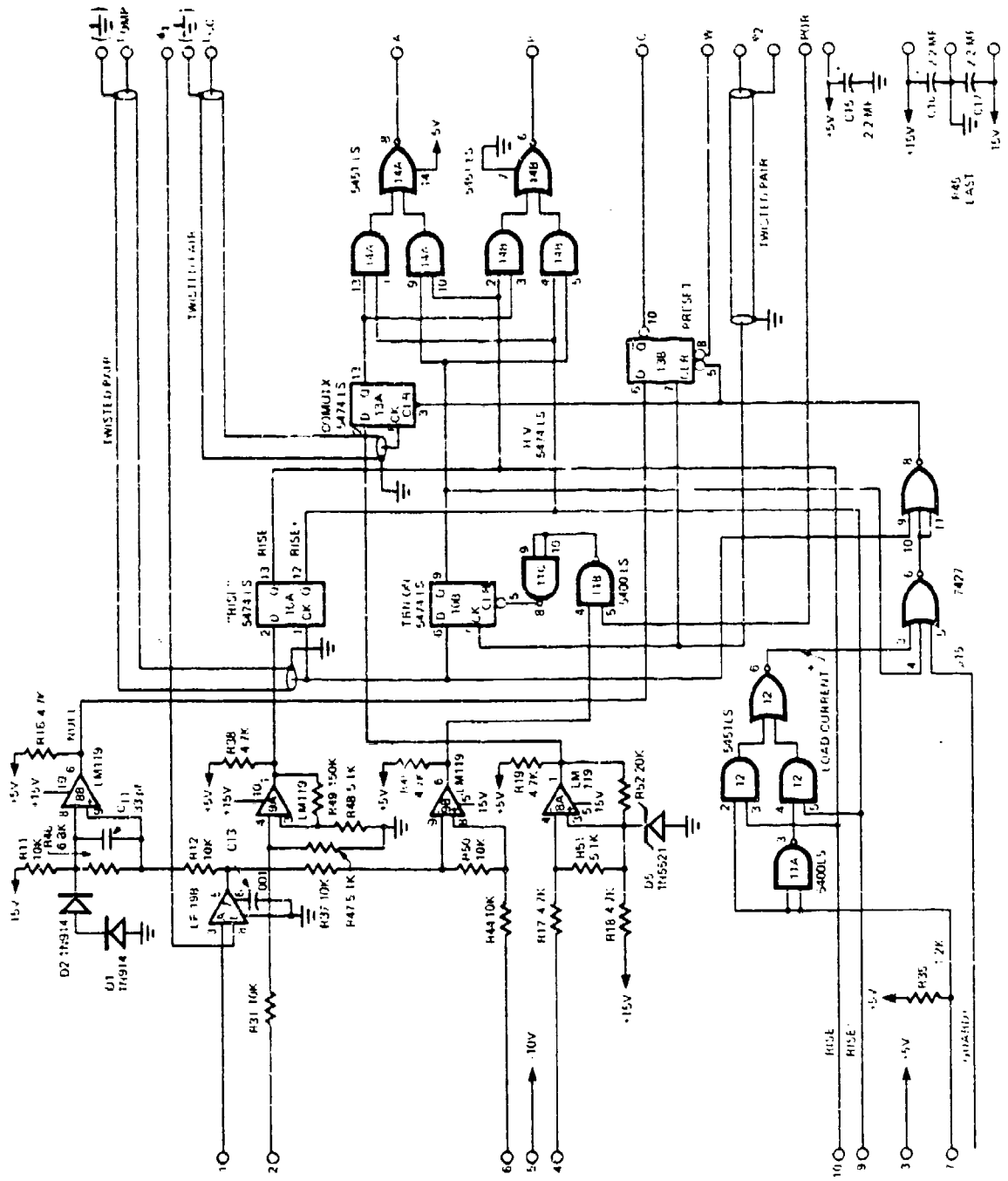
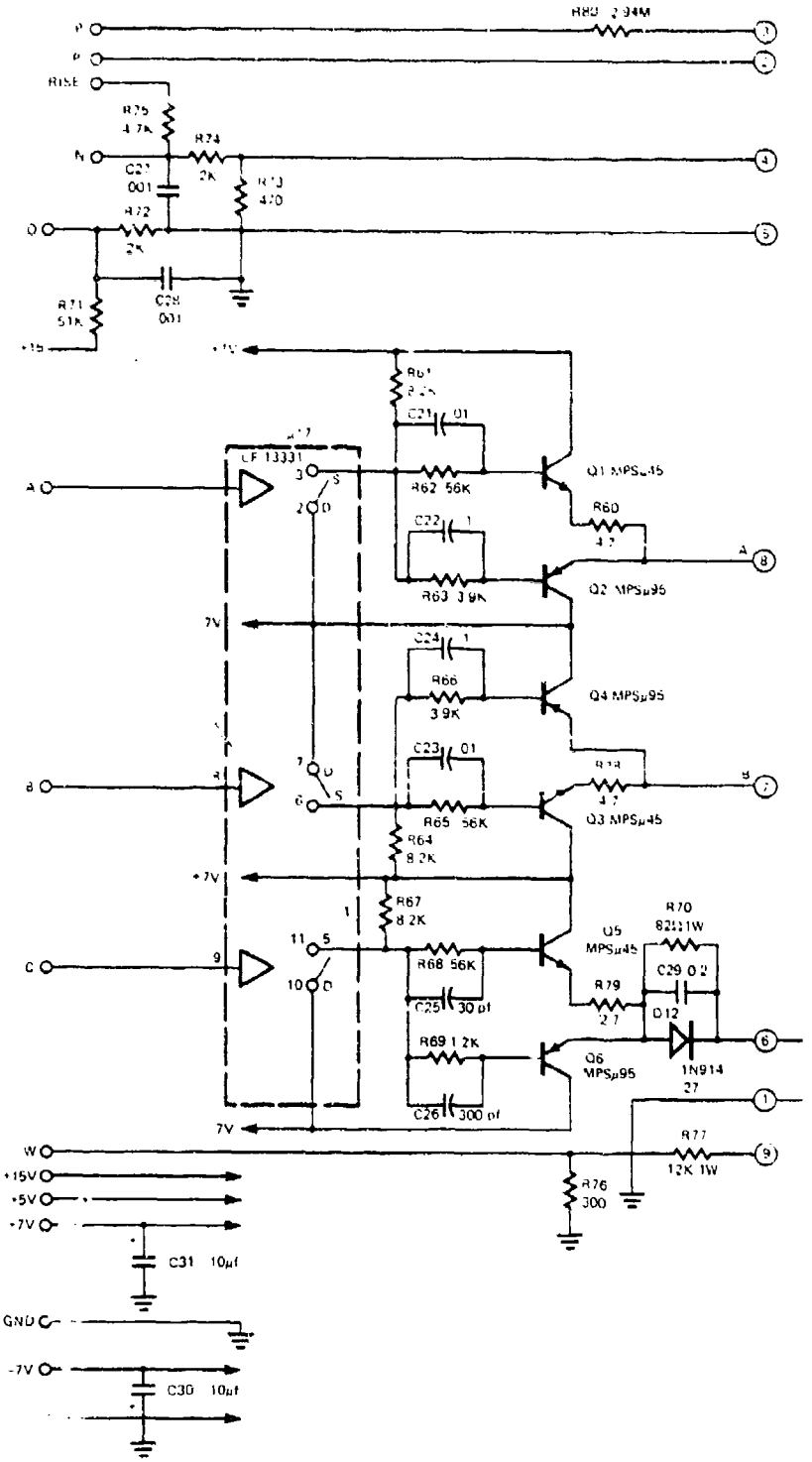


Figure D-3. Logic PC board No. 2 (piggyback) schematic.




e D-4. Main PC board schematic (driver circuits).

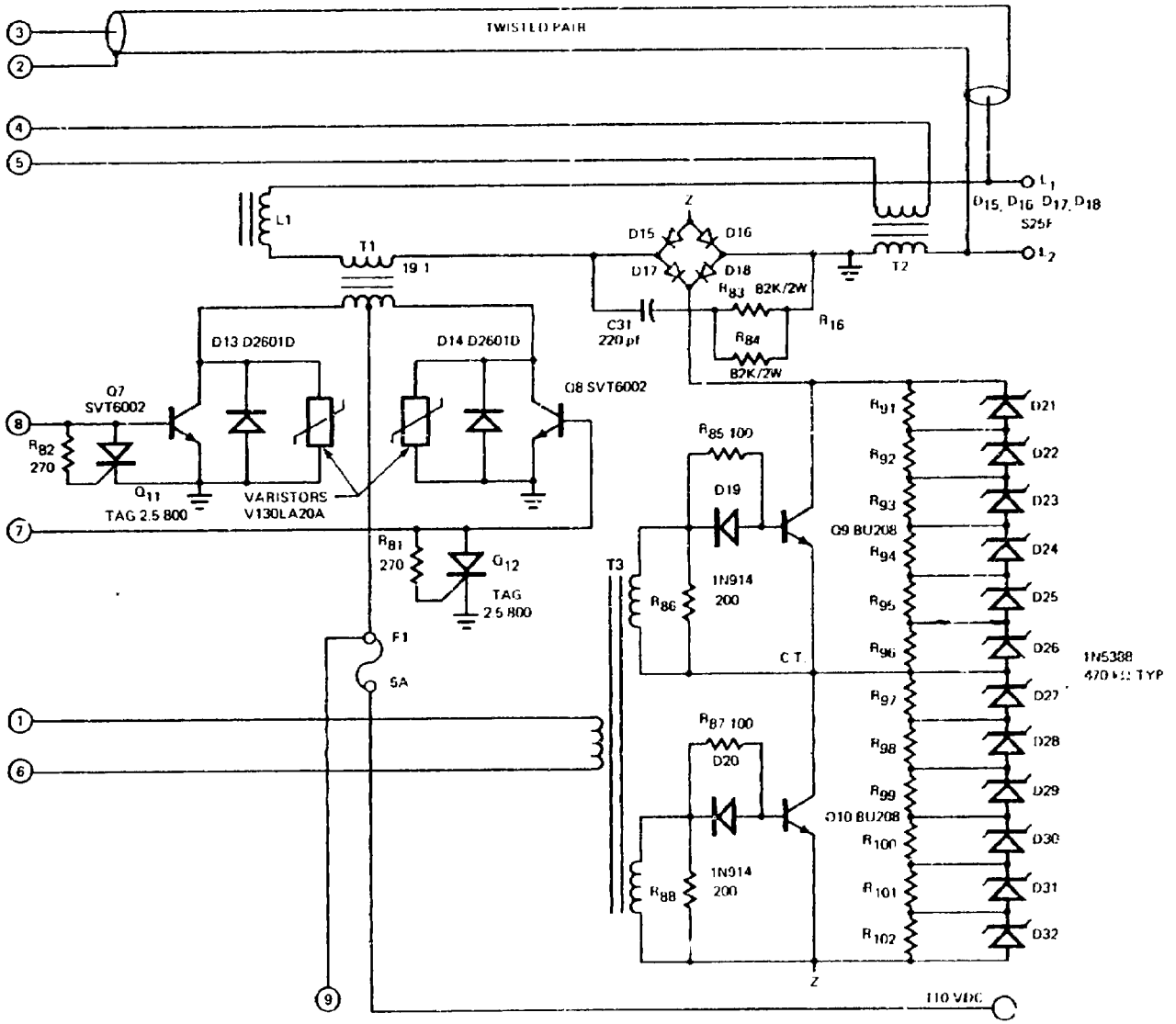



Figure D-5. Heat sink schematic.

# APPENDIX E

## PARTS BREAKDOWN

Logic Breadboard

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| | Printed Wiring Board | A239/61737 | 50125 | 24616-CLB MFR 50125 | Hand-wired breadboard |
| C1 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-CLC1 MFR 93790 | 15 pf |
| C2 | Capacitor (1), Variable, Mica Dielectric | A096/00722 | 72136 | 24616-CLC2 MFR 72136 | 5-25 pf trimmer |
| C3 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-CLC3 MFR 93790 | 5 pf |
| C4 | Capacitor (1), Fixed, Ceramic Dielectric | A010A/00007 | 71590 | 24616-CLC4 MFR | 0.01 µf |
| C5 | Capacitor (1), Fixed, Ceramic Dielectric | A010A/00007 | 71590 | 24616-CLC5 MFR | 0.01 µf |
| C6 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-CLC6 MFR 93790 | 10 pf |
| C7 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-CLC7 93790 | 100 pf |
| C8a | Capacitor (1), Fixed, Ceramic Dielectric | A010A/00007 | 20932 | 24616-CLC8A MFR 20932 | 1 µf |
| C8b | Capacitor (1), Fixed, Electrolytic | A010A/00008 | 93790 | 24616-CLC8B MFR 93790 | 100 µf local deglitch |
| C9 | Capacitor (1), Fixed, Electrolytic | A010A/00008 | 12954 | 24616-CLC9 MFR | 100 µf |

Logic Breadboard (cont.)

| Reference Designation | Name | PIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| C10 | Capacitor (1), Fixed, Ceramic Dielectric | A010A/00007 | 71590 | 24616-CLC10 MFR | 0.01 µf |
| C11 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-CLC11 MFR 93790 | 150 pf |
| C12 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-CLC12 MFR 93790 | 150 pf |
| C13 | Capacitor (1), Fixed, Ceramic Dielectric | A010A/00007 | 71590 | 24616-CLC13 MFR | 0.001 µf |
| C14 | Capacitor (1), Fixed, Plastic Dielectric | A010A/00006 | 93790 | 24616-CLC14 MFR 93790 | 0.001 µf |
| C15 | Capacitor (1), Fixed, Electrolytic | A010A/00008 | 93790 | 24616-CLC15 MFR 93790 | 100 µf 5 V deglitch |
| C16 | Capacitor (1), Fixed, Electrolytic | A010A/00008 | 56289 | 24616-CLC16 MFR 56289 | 100 µf + 15 V deglitch |
| C17 | Capacitor (1), Fixed, Electrolytic | A010A/00008 | 93790 | 24616-CLC17 MFR 93790 | 100 µf -15 V deglitch |
| D1 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-CLD1 MFR | 10 V zener |
| L1 | Coil, Radio Frequency | A058/06338 | 24616 | 24616-CLL1 | 560 µH |

1. Common Logic Breadboard (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R1 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR1 MFR 44655 | 1 K |
| R2 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR2 MFR 44655 | 15 K |
| R3 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR3 MFR 44655 | 470 |
| R4 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR4 MFR 44655 | 27 K |
| R5 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR5 MFR 44655 | 2 K |
| R6 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR6 MFR 44655 | 470 |
| R7 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR7 MFR 44655 | 12 K |
| R8 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR8 MFR 44655 | 2.4 K |
| R9 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR9 MFR 44655 | 1.2 K |
| R10 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR10 MFR 44655 | 1.2 K |
| R11 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR11 MFR 44655 | 51 |

Logic Breadboard (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R12 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR12 MFR 44655 | 51 |
| R13 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR13 MFR 44655 | 2.7 K |
| R14 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR14 MFR 44655 | 1 K |
| R15 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR15 MFR 44655 | 510 |
| R16 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR16 MFR 44655 | 510 |
| R17 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR17 MFR 44655 | 510 |
| R18 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR18 MFR 44655 | 510 |
| R19 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR19 MFR 44655 | 510 |
| R20 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR20 MFR 44655 | 510 |
| R21 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR21 MFR 44655 | 510 |
| R22 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR22 MFR 44655 | 510 |

1. Common Logic Breadboard (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R23 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR23 MFR 44655 | 510 |
| R24 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR24 MFR 44655 | 510 |
| R25 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-CLR25 MFR 44655 | 510 |
| S1 | Switch (1), Toggle | A053/00184 | 32441 | 24616-CLS1 MFR 32441 | |
| U1 | Microcircuit (1), Digital | A458/31779 | 01295 | 24616-CLU1 MFR 01295 | 7411, 3-input AND |
| U2 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-CLU2 MFR | 7410, 3-input NAND |
| U3 | Comparator Module, Signal | A239/61499 | 27014 | 24616-CLU3 MFR | LM319 |
| U9 | Microcircuit (1), Digital | A458/31779 | 01295 | 24616-CLU9 MFR 01295 | 54163, binary counter |
| U10 | Microcircuit (1), Digital | A458/31779 | 01295 | 24616-CLU10 MFR 01295 | 54163, binary counter |

1. Common Logic Breadboard (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| U11 | Microcircuit (1), Digital | A458/31779 | 01295 | 24616-CLU11 MFR 01295 | 54138, 3-8 demaxer |
| U12 | Microcircuit (1), Digital | A458/31779 | 01295 | 24616-CLU12 MFR 01295 | 54154, 4-16 demaxer |
| U13 | Microcircuit (1), Digital | A458/31779 | 01295 | 24616-CLU13 MFR 01295 | 54279, quad latch |
| U16 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-CLU16 MFR | 5438, 2-input driver |
| U17 | Microcircuit (1), Digital | A458/31779 | 04713 | 24616-CLU17 MFR | 7400, 2-input driver |
| U18 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-CLU18 MFR | 5438, 2-input driver |
| U19 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-CLU19 MFR | 5404, hex inverter |
| U21 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-CLU21 MFR | LF 13331, quad analog gate |
| U22 | Microcircuit (1), Linear | A458/31778 | 27014 | 24616-CLU22 MFR | LM 2301, dual op amp |
| Y1 | Oscillator, Radio Frequency | A322/00292 | 01766 | 24616-CLY1 MFR 01766 | 1 MHz crystal |

1. Common Logic Breadboard (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| | Socket, Plug-in Electronic Components | A023/28914 | | 24616-CL200 MFR | DIP Sockets |
| | Cable, Radio Frequency | A077/00779 | 16428 | 24616-W100 MFR 16428 | Miscellaneous shielded cable |
| | Wire, Electrical | A077/00738 | 16428 | 24616-W200 MFR 16428 | Miscellaneous hook-up wire |
| 2. Logic Board #1 | | | | | |
| | Printed Wiring Board | A239/61737 | | 24616-L1PB MFR | Printed circuit Dwg. D1848M109 |
| C1 | Capacitor (1), Fixed, Glass Dielectric | A010A/00004 | 24546 | 24616-L1C1 MFR 24546 | 0.001 µf |
| C2 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-L1C2 MFR 93790 | 150 pf |
| C3 | Capacitor (1), Fixed, Glass Dielectric | A010A/00004 | 24546 | 24616-L1C3 MFR 24546 | 0.1 µf |
| C4 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-L1C4 MFR 93790 | 150 pf |
| C5 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-L1C5 MFR 93790 | 160 pf, integrating cap |
| C6 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-L1C6 MFR 93790 | 20 pf |

2. Logic Board #1 (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| D3 | Semiconductor Device (1), Diode | T327/20589 | 15818 | 24616-L1D3 MFR 15318 | 12 V zener, 1N4742 |
| D4 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-L1D4 MFR | 10 V zener, 1N4740 |
| D8 | Semiconductor Device (1), Diode | T327/20589 | 15818 | 24616-L1D8 MFR 15818 | 15 V zener, 1N5535 |
| D9 | Semiconductor Device (1), Diode | T327/20589 | 15818 | 24616-L1D9 MFR 15818 | 15 V zener, 1N5535 |
| D10 | Semiconductor Device (1), Diode | T327/20589 | 15818 | 24616-L1D10 MFR 15818 | 1N251, rectifier |
| D11 | Semiconductor Device (1), Diode | T327/20589 | 15818 | 24616-L1D11 MFR 15818 | 1N251, rectifier |
| R1 | Resistor (1), Fixed, Film | A001A/05311 | 07716 | 24616-L1R1 MFR 07716 | 20 K 1% |
| R2 | Resistor (1), Fixed, Film | A001A/05311 | 07716 | 24616-L1R2 MFR 07716 | 20 K 1% |
| R3 | Resistor (1), Fixed, Film | A001A/05311 | 07716 | 24616-L1R3 MFR 07716 | 20 K 1% |
| R4 | Resistor (1), Fixed, Film | A001A/05311 | 07716 | 24616-L1R4 MFR 07716 | 20 K 1% |

2. Logic Board #1 (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R5 | Resistor (1), Variable, Nonwire-wound | A002A/29716 | 21030 | 24616-L1R5 MFR 21030 | 1 K, gain adj. |
| R6 | Resistor (1), Fixed, Film | A001A/05311 | 07716 | 24616-L1R6 MFR 07716 | 1.78 K, 1% |
| R7 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R7 MFR 44655 | 82 K |
| R8 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R8 MFR 44655 | 100 K |
| R9 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R9 MFR 44655 | 51 K |
| R10 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R10 MFR 44655 | 51 K |
| R13 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R13 MFR 44655 | 120 K |
| R14 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R14 MFR 44655 | 120 K |
| R15 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R15 MFR 44655 | 4.7 K |
| R20 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R20 MFR 44655 | 82 K |
| R21 | Resistor (1), Variable, Nonwire | A002A/29716 | 21030 | 24616-L1R21 MFR 21030 | 50 K, offset adj. |

2. Logic Board #1 (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R22 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R22 MFR 44655 | 100 K |
| R23 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R23 MFR 44655 | 680 K |
| R24 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R24 MFR 44655 | 43 K |
| R25 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R25 MFR 44655 | 910 K |
| R26 | Resistor (1), Fixed, Film | A001A/05311 | 07716 | 24616-L1R26 MFR 07716 | 20 K, 1% |
| R27 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R27 MFR 44655 | 15 K |
| R28 | Resistor (1), Fixed, Film | A001A/05311 | 07716 | 24616-L1R28 MFR 07716 | 20 K, 1% |
| R29 | Resistor (1), Fixed, Film | A001A/05311 | 07716 | 24616-L1R29 MFR 07716 | 20 K, 1% |
| R30 | Resistor (1), Fixed, Film | A001A/05311 | 07716 | 24616-L1R30 MFR 07716 | 10 K, 1% |
| R32 | Resistor (1), Fixed, Film | A001A/05311 | 07716 | 24616-L1R32 MFR 07716 | 20 K, 1% |
| R33 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R33 MFR 44655 | 5.1 K |

2. Logic Board #1 (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R36 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R36 MFR 44655 | 33 K |
| R39 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R39 MFR 44655 | 2.7 K |
| R40 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R40 MFR 44655 | 1.5 K |
| R41 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R41 MFR 44655 | 510 |
| R42 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R42 MFR 44655 | 430 |
| R43 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R43 MFR 44655 | 6.2 K |
| R53 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R53 MFR 44655 | 150 K |
| R55 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R55 MFR 44655 | 20 K |
| R56 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L1R56 MFR 44655 | 2 K |
| U1 | Microcircuit (1), Linear | A458/31778 | 27014 | 24616-L1U1 MFR | LM 124, quad op amp |
| U2 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-L1U2 MFR | LF 13331, quad analog gate |

2. Logic Board #1 (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| U3 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-L1U3 MFR | LF 13231, |
| U4 | Comparator Module, Signal | A239/61499 | 27014 | 24616-L1U4 MFR | LM 119, dual comparator |
| U5 | Microcircuit (1), Linear | A458/31778 | 27014 | 24616-L1U5 MFR | LF 398, sample-hold amp |
| U6 | Microcircuit (1), Linear | A458/31778 | 27014 | 24616-L1U6 MFR | LH2101A, dual op amp |
| U16 | Microcircuit (1), Linear | A458/31778 | 27014 | 24616-L1U16 MFR | LM 201, op amp |

3. Logic Board #2 (Piggy Back)

| | | | | | |
|---|---|---|---|---|---|
| | Printed Wiring Board | A239/61737 | | 24616-L2PB MFR | Printed circuit Dwg. D1848M110 |
| C11 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-L2C11 MFR 93790 | 33 pf |
| C13 | Capacitor (1), Fixed, Glass Dielectric | A010A/00004 | 24546 | 24616-L2C13 MFR 24546 | 0.1 µf |
| C15 | Capacitor (1), Fixed, Electrolytic | A010A/00008 | 12954 | 24616-L2C15 MFR | 33 µf 5 V deglitch |

3. Logic Board #2 (Piggy Back) (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| C16 a | Capacitor (1), Fixed, Ceramic Dielectric | A010A/00007 | 20932 | 24616-L2C16A MFR 20932 | 1 µf 15 V deglitch |
| C16 b | Capacitor (1), Fixed, Ceramic Dielectric | A010A/00007 | 20932 | 24616-L2C16B MFR 20932 | 1 µf 15 V deglitch |
| C17 | Capacitor (1), Fixed, Ceramic Dielectric | A010A/00007 | 20932 | 24616-L2C17 MFR 20932 | 1 µf -15 V deglitch |
| D1 | Semiconductor Device (1), Diode | T327/20589 | 07263 | 24616-L2D1 MFR | 1N914 |
| D2 | Semiconductor Device (1), Diode | T327/20589 | 07263 | 24616-L2D2 MFR | 1N914 |
| R11 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R11 MFR 44655 | 10 K |
| R12 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R12 MFR 44655 | 10 K |
| R16 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R16 MFR 44655 | 4.7 K |
| R17 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R17 MFR 44655 | 4.7 K |
| R18 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R18 MFR 44655 | 4.7 K |
| R19 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R19 MFR 44655 | 4.7 K |

3. Logic Board #2 (Piggy Back) (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R31 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R31 MFR 44655 | 10 K |
| R37 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R37 MFR 44655 | 10 K |
| R38 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R38 MFR 44655 | 4.7 K |
| R44 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R44 MFR 44655 | 10 K |
| R45 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R45 MFR 44655 | 4.7 K |
| R46 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R46 MFR 44655 | 6.8 K |
| R47 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R47 MFR 44655 | 5.1 K |
| R48 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R48 MFR 44655 | 5.1 K |
| R49 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R49 MFR 44655 | 150 K |
| R50 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R50 MFR 44655 | 10 K |
| R51 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R51 MFR 44655 | 5.1 K |

3. Logic Board #2 (Piggy Back) (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R52 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-L2R52 MFR 44655 | 20 K |
| U7 | Microcircuit (1), Linear | A458/31778 | 27014 | 24616-L2U7 MFR | LF398, sample-hold amp |
| U8 | Comparator Module, Signal | A239/61499 | 27014 | 24616-L2U8 MFR | LM119, dual comparator |
| U9 | Comparator Module, Signal | A239/61499 | 27014 | 24616-L2U9 MFR | LM119, dual comparator |
| U10 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-L2U10 MFR | 5474LS, dual flip flop |
| U11 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-L2U11 MFR | 5400LS, quad NAND |
| U12 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-L2U12 MFR | 5451LS, AND-OR-INVERT |
| U13 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-L2U13 MFR | 5474LS, dual flip flop |
| U14 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-L2U14 MFR | 5451LS, dual AND-OR-INVERT |
| U15 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-L2U15 MFR | 7427, triple NOR |
| | Wire, Electrical | A077/00798 | 16428 | 24616-L2W00 MFR 16428 | #28 wire for twisted pairs |

4. Main Simplifier PC Board (Driver Board) (not including heat sink and mounted components)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| | Printed Wiring Board | A239/61737 | | 24616-MDPB | Printed circuit Dwg. D1848M111 |
| C21 | Capacitor (1), Fixed, Glass Dielectric | A010A/00004 | 24546 | 24616-MDC21 MFR 24546 | 0.01 µf |
| C22 | Capacitor (1), Fixed, Glass Dielectric | A010A/00004 | 24546 | 24616-MDC22 MFR 24546 | 0.1 µf |
| C23 | Capacitor (1), Fixed, Glass Dielectric | A010A/00004 | 24546 | 24616-MDC23 MFR 24546 | 0.01 µf |
| C24 | Capacitor (1), Fixed, Glass Dielectric | A010A/00004 | 24546 | 24616-MDC24 MFR 24546 | 0.1 µf |
| C25 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-MDC25 MFR 93790 | 30 pf |
| C26 | Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 93790 | 24616-MDC26 MFR 93790 | 300 pf |
| C27 | Capacitor (1), Fixed, Plastic Dielectric | A010A/00006 | 56289 | 24616-MDC27 MFR 56289 | 0.001 µf |
| C28 | Capacitor (1), Fixed, Plastic Dielectric | A010A/00006 | 56289 | 24616-MDC28 MFR 56289 | 0.001 µf |
| C29 | Capacitor (1), Fixed, Plastic Dielectric | A010A/00006 | | 24616-MDC29 MFR | 0.2 µf, Midwec |
| C30 | Capacitor (1), Fixed, Electrolytic | A010A/00008 | 12954 | 24616-MDC30 MFR | 33 µf +7 V deglitch |

4. Main Simplifier PC Board (Driver Board) (not including heat sink and mounted components) (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| C31 | Capacitor (1), Fixed, Electrolytic | A010A/00008 | 12954 | 24616-MDC31 MFR | 33 µf -7 V deglitch |
| D12 | Semiconductor Device (1), Diode | T327/20589 | 07263 | 24616-MDD12 MFR | 1N914 |
| Q1 | Transistor | T327/20588 | 04713 | 24616-MDQ1 MFR | MPS µ 45 (NPN) |
| Q2 | Transistor | T327/20588 | 04713 | 24616-MDQ2 MFR | MPS µ 95 (PNP) |
| Q3 | Transistor | T327/20588 | 04713 | 24616-MDQ3 MFR | MPS µ 45 (NPN) |
| Q4 | Transistor | T327/20588 | 04713 | 24616-MDQ4 MFR | MPS µ 95 (PNP) |
| Q5 | Transistor | T327/20588 | 04713 | 24616-MDQ5 MFR | MPS µ 45 (NPN) |
| Q6 | Transistor | T327/20588 | 04713 | 24616-MDQ6 MFR | MPS µ 95 (PNP) |
| R60 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR60 MFR 44655 | 4.7 Ω,1 W |
| R61 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR61 MFR 44655 | 8.2 K |
| R62 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR62 MFR 44655 | 56 K |

4. Main Simplifier PC Board (Driver Board) (not including heat sink and mounted components) (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R63 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR63 MFR 44655 | 3.9 K |
| R64 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR64 MFR 44655 | 8.2 K |
| R65 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR65 MFR 44655 | 56 K |
| R66 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR66 MFR 44655 | 3.9 K |
| R67 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR67 MFR 44655 | 8.2 K |
| R68 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR68 MFR 44655 | 56 K |
| R69 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR69 MFR 44655 | 1.2 K |
| R70 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR70 MFR 44655 | 82 Ω, 1 W |
| R71 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR71 MFR 44655 | 51 K |
| R72 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR72 MFR 44655 | 2 K |
| R73 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR73 MFR 44655 | 470 |

4. Main Simplifier PC Board (Driver Board) (not including heat sink and mounted components) (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R74 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR74 MFR 44655 | 2 K |
| R75 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR75 MFR 44655 | 4.7 K |
| R76 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR76 MFR 44655 | 300 |
| R77 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR77 MFR 44655 | 12 K, 1 W |
| R78 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR78 MFR 44655 | 4.7 Ω,1 W |
| R79 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MDR79 MFR 44655 | 2.7 Ω 1 W |
| R80 | Resistor (1), Fixed, Film | A001A/05311 | 91637 | 24616-MDR80 MFR 91637 | 2.94 M 1% carbon film |
| U17 | Microcircuit (1), Digital | A458/31779 | 27014 | 24616-MDU17 MFR | LF 13331 quad analog gate |

5. Heat Sink and Mounted Components

| | | | | |
|---|---|---|---|---|
| Heat Sink, Electrical - Electronic Component | A239/61433 | 24616 | 24616-MHH | Dwg. |
| Terminal (1), Stud | A006A/00887 | | 24616-MHS MFR | H. H. Smith - insulated terms. |

5. Heat Sink and Mounted Components (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| D13 | Semiconductor Device (1), Diode | T327/20589 | 07235 | 24616-MHD13 MFR RCA | D2601D, free-wheeling diode |
| D14 | Semiconductor Device (1), Diode | T327/20589 | 07235 | 24616-MHD14 MFR RCA | D2601D, free-wheeling diode |
| D15 | Semiconductor Device (1), Diode | T327/20589 | 50891 | 24616-MHD15 MFR 50891 | S25F, high-voltage diode |
| D16 | Semiconductor Device (1), Diode | T327/20589 | 50891 | 24616-MHD16 MFR 50891 | S25F, high-voltage diode |
| D17 | Semiconductor Device (1), Diode | T327/20589 | 50891 | 24616-MHD17 MFR 50891 | S25F, high-voltage diode |
| D18 | Semiconductor Device (1), Diode | T327/20589 | 50891 | 24616-MHD18 MFR 50891 | S25F, high-voltage diode |
| D19 | Semiconductor Device (1), Diode | T327/20589 | 07263 | 24616-MHD19 MFR | 1N914 |
| D20 | Semiconductor Device (1), Diode | T327/20589 | 07263 | 24616-MHD20 MFR | 1N914 |
| D21 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD21 MFR | 1N5388, 200 V zener |
| D22 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD22 MFR | 1N5388, 200 V zener |
| D23 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD23 MFR | 1N5388, 200 V zener |

5. Heat Sink and Mounted Components (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| D24 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD24 MFR | IN5388, 200 V zener |
| D25 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD25 MFR | IN5388, 200 V zener |
| D26 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD26 MFR | IN5388, 200 V zener |
| D27 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD27 MFR | IN5388, 200 V zener |
| D28 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD28 MFR | IN5388, 200 V zener |
| D29 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD29 MFR | IN5388, 200 V zener |
| D30 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD30 MFR | IN5388, 200 V zener |
| D31 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD31 MFR | IN5388, 200 V zener |
| D32 | Semiconductor Device (1), Diode | T327/20589 | 04713 | 24616-MHD32 MFR | IN5388, 200 V zener |
| | Semiconductor Device (1), Diode | T327/20589 | 09214 | 24616-MHD33 MFR | Varistor V130LA20A |
| | Semiconductor Device (1), Diode | T327/20589 | 09214 | 24616-MHD34 MFR | Varistor V130LA20A |

5. Heat Sink and Mounted Components (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| F1 | Fuse (1), Cartridge | A017/00248 | 54426 | 24616-MHF1 MFR 54426 | 3 AG type, 5A |
| | Fuseholder (1), Block | A014A/28908 | 54426 | 24616-MHFX MFR 54426 | |
| L1 | Coil, Radio Frequency | A058/06338 | 24616 | 24616-MHL1 | 13 mH, charging inductor |
| Q7 | Transistor | T327/20588 | 01281 | 24616-MHQ7 MFR TRW | SVT 6002, PS transistor |
| Q8 | Transistor | T327/20588 | 01281 | 24616-MHQ8 MFR TRW | SVT 6002, PS transistor |
| Q9 | Transistor | T327/20588 | 04713 | 24616-MHQ9 MFR | BU208, HVG transistor |
| Q10 | Transistor | T327/20588 | 04713 | 24616-MHQ10 MFR | BU208, HVG transistor |
| Q11 | Transistor | T327/20588 | | 24616-MHQ11 MFR | SCR, 2.5 - 800 (TAG) |
| Q12 | Transistor | T327/20588 | | 24616-MHQ12 MFR | SCR, 2.5 - 800 (TAG) |
| R81 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR81 MFR 44655 | 270 Ω |

5. Heat Sink and Mounted Components (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R82 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR82 MFR 44655 | 270 Ω |
| R83 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR83 MFR 44655 | 82 K, 2 W |
| R84 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR84 MFR 44655 | 82 K, 2 W |
| R85 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR85 MFR 44655 | 100 Ω |
| R86 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR86 MFR 44655 | 200 Ω |
| R87 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR87 MFR 44655 | 100 Ω |
| R88 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR88 MFR 44655 | 200 Ω |
| R89 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR89 MFR 44655 | 470 kΩ |
| R90 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR90 MFR 44655 | 470 kΩ |
| R91 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR91 MFR 44655 | 470 kΩ |
| R92 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR92 MFR 44655 | 470 kΩ |

5. Heat Sink and Mounted Components (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| R93 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR93 MFR 44655 | 470 kΩ |
| R94 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR94 MFR 44655 | 470 kΩ |
| R95 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR95 MFR 44655 | 470 kΩ |
| R96 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR96 MFR 44655 | 470 kΩ |
| R97 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR97 MFR 44655 | 470 kΩ |
| R98 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR98 MFR 44655 | 470 kΩ |
| R99 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR99 MFR 44655 | 470 kΩ |
| R100 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR100 MFR 44655 | 470 kΩ |
| R101 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR101 MFR 44655 | 470 kΩ |
| R102 | Resistor (1), Fixed, Composition | A001A/00126 | 44655 | 24616-MHR102 MFR 44655 | 470 kΩ |
| T1 | Transformer, Power, Step-up | A058/00756 | 24616 | 24616-MHT1 | Main transformer |

5. Heat Sink and Mounted Components (cont.)

| Reference Designation | Name | FIIG | Manufacturers' Code | Part No. | Remarks |
|---|---|---|---|---|---|
| T2 | Transformer, Current | A058/00738 | 24616 | 24616-MHT2 | |
| T3 | Transformer, Pulse | A058/00208 | 24616 | 24616-MHT3 | HVG base driver transformer |
| | Wire, Electrical | A077/00798 | 16428 | 24616-MHW0 MFR 16428 | Hook-up wire (teflon coated) |
| | Capacitor (1), Fixed, Electrolytic | A010A/00008 | 56289 | 24616-MHC32 MFR 56289 | 40 µf - 450 V 112 V, storage (2 ea.) |
| | Capacitor (1), Fixed, Electrolytic | A010A/00008 | | 24616-MHC34 MFR | 1000 µf -7 V deglitch |
| | Capacitor (1), Fixed, Electrolytic | A010A/00008 | | 24616-MHC35 MFR | 2200 µf +7 V deglitch |

6. The Load

| | | | | |
|---|---|---|---|---|
| Capacitor (1), Fixed, Mica Dielectric | A010A/00005 | 99120 | 24616-XC1 MFR 99120 | (1 ea.) |
| Capacitor (1), Fixed, Ceramic Dielectric | A010A/00007 | 56289 | 24616-XC2 MFR 56289 | (3 ea.) |
| Wire, Electrical | A077/00798 | 16428 | 24616-XW0 MFR 16428 | Hook-up wire (twisted pair) |

# APPENDIX F

# OPERATING INSTRUCTIONS

The breadboard/prototype assembly should be operated only with a specified load of 0.05 μf capacitance and at a sufficient working voltage rating, or a PZ stack of proper capacitance and voltage rating.

It is possible to operate one channel at a time by pulling the fuse of the other. These fuses, when installed, should have a rating of 5 A. Slo-blo or MDL types should not be used. It is to be noted that logic power, including +7 V and -7 V, still reaches a channel even if the fuse is pulled.

It is recommended that regulated power supplies be used with current limits, and these current limits be set to the maximum current draw ratings listed in Table 1.

When powering up the assembly, the +5 V, -10 V, +15 V, and -15 V power supplies should first be turned on; then the +7 V and -7 V supplies should be turned on. Finally the 112 V power supply should be turned on. When powering down, the reverse sequence should be followed.

In its present status, channel 8 should be operated only up to ±1325 V, and both channels should not have step commands of and greater than ±1200 V. Also, it is suggested that when powering up, signals of zero or nearly zero volts prevail.

# APPENDIX G

# CALIBRATION

Since the actuator amplifier prototype breadboard has a specified gain of 150 and an offset of zero, but is provided with gain and offset trimpot adjustments, a procedure is necessary for bringing the actuator amplifier to its specifications.

The two channels are adjusted independently. Each is provided with a gain adjustment trimpot and an offset adjustment trimpot. Each is a multiturn screwdriver-adjustment trimpot.

Calibration Procedure:

1. Support the logic-piggyback assembly by suitable means so that the act of adjusting the trimpots does not short out clip leads bringing in signals;

2. With suitable loads connected, power up breadboard;

3. Ground input No. 7 by clipleading its signal lead to its local ground lead (do not use other ground terminal posts);

4. Adjust $R_{21}$ (see Figure G-1) so as to bring output to 0 V (±15 V);

5. Apply 8.00 V to the input, increasing it slowly to the 8 V so as to avoid applying much greater than 8 V;

6. Adjust $R_5$ so as to bring output to 1200 V (±15 V);

7. Repeat steps 3 through 6 for channel 8.

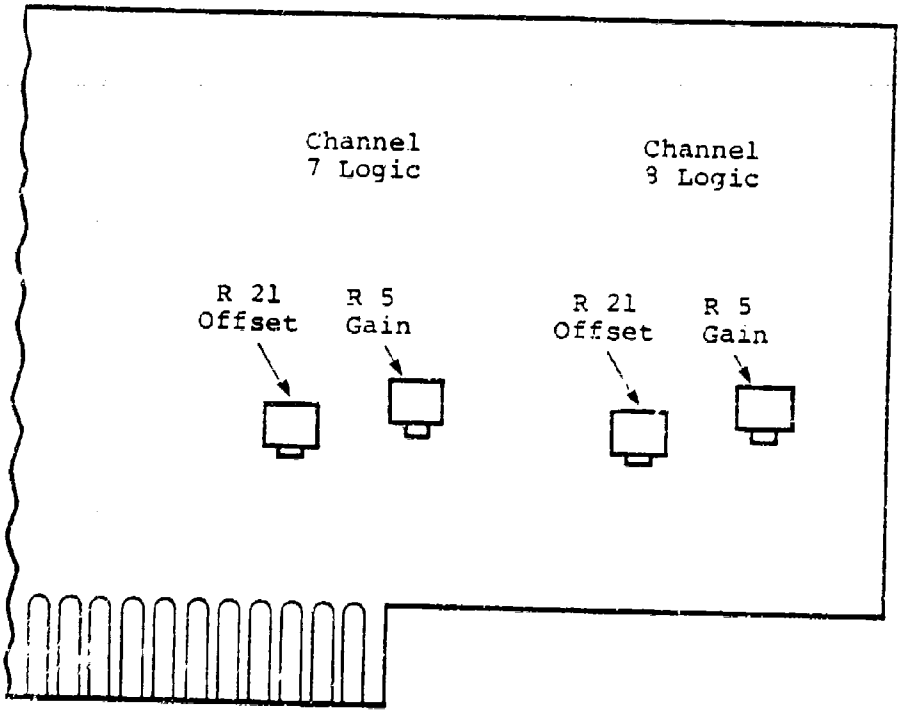



Figure C-1. Location of calibrating trimpots on logic PC board.

# APPENDIX H

# LIST OF TAPES

## LIST OF TAPES

Following are the contents of the tapes made during the contractural tests. The tapes recorded are labeled in sequence. Each tape has 20 files. One file holds 1 array on the Norland. Up to four files can be recorded at one time. Tapes are recorded on the A-side only, except as noted.

| Tape | File | Channel | Test | |
|---|---|---|---|---|
| 1 | 1 | 7 | 1A | 0 V, output |
| 1 | 2 | 7 | 1A | 0 V, input |
| 1 | 3 | 7 | 1B | 500 V, output |
| 1 | 4 | 7 | 1B | 500 V, input |
| 1 | 5 | 7 | 1C | 1000 V, output |
| 1 | 6 | 7 | 1C | 1000 V, input |
| 1 | 7 | 7 | 1D | 1500 V, output |
| 1 | 8 | 7 | 1D | 1500 V, input |
| 1 | 9 | 8 | 1A | 0 V, output |
| 1 | 10 | 8 | 1A | 0 V, input |
| 1 | 11 | 8 | 1B | 500 V, output |
| 1 | 12 | 8 | 1B | 500 V, input |
| 1 | 13 | 8 | 1C | 1000 V, output |
| 1 | 14 | 8 | 1C | 1000 V, input |
| 1 | 15 | 8 | 1D | 1500 V, output |
| 1 | 16 | 8 | 1D | 1500 V, input |
| 1 | 17 | 7 | 2A | output |
| 1 | 18 | 7 | 2A | input |
| 1 | 19 | 7 | 2B | output |
| 1 | 20 | 7 | 2B | input |
| 2 | 1 | 7 | 2C | output |
| 2 | 2 | 7 | 2C | input |
| 2 | 3 | 7 | 2D | output |
| 2 | 4 | 7 | 2D | input |
| 2 | 5 | 7 | 2E | output |
| 2 | 6 | 7 | 2E | input |
| 2 | 7 | 7 | 2F | output |
| 2 | 8 | 7 | 2F | input |
| 2 | 9 | 7 | 2G | output |
| 2 | 10 | 7 | 2G | input |
| 2 | 11 | 7 | 2H | output |
| 2 | 12 | 7 | 2H | input |
| 2 | 13 | 7 | 2J | output |
| 2 | 14 | 7 | 2J | input |

| Tape | File | Channel | Test | |
|---|---|---|---|---|
| 2 | 15 | 8 | 2A | output |
| 2 | 16 | 8 | 2A | input |
| 2 | 17 | 8 | 2B | output |
| 2 | 18 | 8 | 2B | input |
| 2 | 19 | Calculating program for linearity, slope, and standard deviation stored here. | | |
| 3 | 1 | 8 | 2C | output |
| 3 | 2 | 8 | 2C | input |
| 3 | 3 | 8 | 2D | output |
| 3 | 4 | 8 | 2D | input |
| 3 | 5 | 8 | 2E | output |
| 3 | 6 | 8 | 2E | input |
| 3 | 7 | 8 | 2F | output |
| 3 | 8 | 8 | 2F | input |
| 3 | 9 | 8 | 2G | output |
| 3 | 10 | 8 | 2G | input |
| 3 | 11 | 8 | 2H | output |
| 3 | 12 | 8 | 2H | input |
| 3 | 13 | 8 | 2J | output |
| 3 | 14 | 8 | 2J | input |
| 3 | 15 | 7 | 3A | output |
| 3 | 16 | 7 | 3A | input |
| 3 | 17 | 7 | 3B | output |
| 3 | 18 | 7 | 3B | input |
| 3 | 19 | 7 | 3C | output |
| 3 | 20 | 7 | 3C | input |
| 4 | 1 | 7 | 3D | output |
| 4 | 2 | 7 | 3D | input |
| 4 | 3 | 7 | 3E | output |
| 4 | 4 | 7 | 3E | input |
| 4 | 5 | 7 | 3F | output |
| 4 | 6 | 7 | 3F | input |
| 4 | 7 | 7 | 3G | output |
| 4 | 8 | 7 | 3G | input |
| 4 | 9 | 7 | 3H | input |
| 4 | 10 | 7 | 3H | input |
| 4 | 11 | 8 | 3A | output |
| 4 | 12 | 8 | 3A | input |
| 4 | 13 | 8 | 3B | output |
| 4 | 14 | 8 | 3B | input |
| 4 | 15 | 8 | 3C | output |
| 4 | 16 | 8 | 3C | input |
| 4 | 17 | 8 | 3D | output |
| 4 | 18 | 8 | 3D | input |
| 4 | 19 | 8 | 3E | output |
| 4 | 20 | 8 | 3E | input |
| 5 | 1 | 8 | 3F | output |
| 5 | 2 | 8 | 3F | input |
| 5 | 3 | 8 | 3G | output |
| 5 | 4 | 8 | 3G | input |

| Tape | File | Channel | Test | |
|---|---|---|---|---|
| 5 | 5 | 8 | 3H | output |
| 5 | 6 | 8 | 3H | input |
| 5 | 7 | 7 | 4A | output |
| 5 | 8 | 7,8 | 4A | input |
| 5 | 9 | 8 | 4A | output |
| 5 | 10 | 7 | 4B | output |
| 5 | 11 | 7,8 | 4B | input |
| 5 | 12 | 8 | 4B | output |
| 5 | 13 | 7 | 4C | output |
| 5 | 14 | 7,8 | 4C | input |
| 5 | 15 | 8 | 4C | output |
| 5 | 16 | 7 | 4D | output |
| 5 | 17 | 7,8 | 4D | input |
| 5 | 18 | 8 | 4D | output |
| 6 | 1 | 7 | 4E | output |
| 6 | 2 | 7,8 | 4E | input |
| 6 | 3 | 8 | 4E | output |
| 6 | 4 | 7 | 4F | output |
| 6 | 5 | 7,8 | 4F | input |
| 6 | 6 | 8 | 4F | output |
| 6 | 7 | 7 | 4G | output |
| 6 | 8 | 7,8 | 4G | input |
| 6 | 9 | 8 | 4G | output |
| 6 | 10 | 7 | 4H | output |
| 6 | 11 | 7,8 | 4H | input |
| 6 | 12 | 8 | 4H | output |
| 6 | 13 | 7 | 4J | output |
| 6 | 14 | 7,8 | 4J | input |
| 6 | 15 | 8 | 4J | output |
| 6 | 16 | 7 | 4K | input |
| 6 | 17 | 7 | 4K | output |
| 6 | 18 | 7 | 4L | input |
| 6 | 19 | 7 | 4L | output |
| 6 | 20 | Calculating program for sine wave data reduction stored here. | | |

| Tape | File | Channel | Test | |
|---|---|---|---|---|
| 7 | 1 | 7 | 4M | input |
| 7 | 2 | 7 | 4M | output |
| 7 | 3 | 7 | 4N | input |
| 7 | 4 | 7 | 4N | output |
| 7 | 5 | 7 | 4P | input |
| 7 | 6 | 7 | 4P | output |
| 7 | 7 | 7 | 4Q | input |
| 7 | 8 | 7 | 4Q | output |
| 7 | 9 | 7 | 4R | input |
| 7 | 10 | 7 | 4R | output |
| 7 | 11 | 7 | 4S | input (200 Hz) |
| 7 | 12 | 7 | 4S | output (200 Hz) |
| 7 | 13 | 7 | 4T | input (500 Hz) |
| 7 | 14 | 7 | 4T | output (500 Hz) |
| 7 | 15 | 7 | 4U | input (1 kHz) |
| 7 | 16 | 7 | 4U | output (1 kHz) |
| 7 | 17 | 8 | 4K | input |
| 7 | 18 | 8 | 4K | output |
| 7 | 19 | 8 | 4L | output |
| 7 | 20 | 8 | 4L | input |
| 8 | 1 | 8 | 4M | output |
| 8 | 2 | 8 | 4M | input |
| 8 | 3 | 8 | 4N | output |
| 8 | 4 | 8 | 4N | input |
| 8 | 5 | 8 | 4P | output |
| 8 | 6 | 8 | 4P | input |
| 8 | 7 | 8 | 4Q | output |
| 8 | 8 | 8 | 4Q | input |
| 8 | 9 | 8 | 4R | output |
| 8 | 10 | 8 | 4R | input |
| 8 | 11 | 8 | 4S | output (200 Hz) |
| 8 | 12 | 8 | 4S | input (200 Hz) |

| Tape | File | Channel | Test | |
|---|---|---|---|---|
| 8 | 13 | 8 | 4T | output (500 Hz) |
| 8 | 14 | 8 | 4T | input (500 Hz) |
| 8 | 15 | 8 | 5A | output |
| 8 | 16 | 8 | 5A | input |
| 8 | 17 | 7 | 5A | input |
| 8 | 18 | 7 | 5A | output |
| 9A | 1 | 8 | 5B | output |
| 9A | 2 | 8 | 5B | input |
| 9A | 3 | 7 | 5B | input |
| 9A | 4 | 7 | 5B | output |
| 9A | 5 | 8 | 5C | output (+2.5 V, +5 V) |
| 9A | 6 | 8 | 5C | input (+2.5 V, +5 V) |
| 9A | 7 | 7 | 5C | input (+2.5 V, +5 V) |
| 9A | 8 | 7 | 5C | output (+2.5 V, +5 V) |
| 9A | 9 | (blank) | | |
| 9A | 10 | (blank) | | |
| 9A | 11 | 8 | 5D | output |
| 9A | 12 | 8 | 5D | input |
| 9A | 13 | 7 | 5D | input |
| 9A | 14 | 7 | 5D | output |
| 9A | 15 | 8 | 5E | output |
| 9A | 16 | 8 | 5E | input |
| 9A | 17 | 7 | 5E | input |
| 9A | 18 | 7 | 5E | output |
| 9A | 19 | (blank) | | |
| 9A | 20 | (blank) | | |
| 9B | 1 | 8 | 5F | output |
| 9B | 2 | 8 | 5F | input |
| 9B | 3 | 7 | 5F | output |
| 9B | 4 | 7 | 5F | input |
| 9B | 5 | 8 | 5G | output |
| 9B | 6 | 8 | 5G | input |
| 9B | 7 | 7 | 5G | output |
| 9B | 8 | 8 | 6 | output - initial |
| 9B | 9 | 8 | 6 | input - initial |
| 9B | 10 | 7 | 6 | output - initial |
| 9B | 11 | 7 | 6 | input - initial |
| 9B | 12 | 8 | 6 | output - final |
| 9B | 13 | 8 | 6 | input - final |
| 9B | 14 | 7 | 6 | output - final |
| 9B | 15 | 7 | 6 | input - final |

# APPENDIX I

# NORLAND DATA REDUCTION PROGRAMS

The programs written below for the Norland NI1200A Programmable Calculating Oscilloscope (PCO) are presented here in the abbreviated key-syntax described in the Norland PCO Operating Manual.

The program below allows the Norland PCO to determine the slope, standard deviation voltage, and linearity of a ramp being held in a display array. To run the program, put the P cursor near the beginning, but within the ramp to be analyzed and the Q cursor near the end but within. When the program ends, m (slope) is on E, $V_d$ (standard deviation voltage) is on B' and $\sigma$ (linearity) is on C'. $\sigma$ is referenced to $\Delta V$, the difference of the two initial cursor voltages.

```
O . ⟶ B'
O . ⟶ C'
O . ⟶ D'
COOR
V ⟶ A
T ⟶ B
ΔCOOR
V ⟶ C
T ⟶ D
C / D ⟶ E
P ⟶
ΔCOOR
T IF> C'
COOR
```

```
A' * E ⟶ A'
A' + A ⟶ A'
V - A' ⟶ A'
A' * A' ⟶ A'
B' + A' ⟶ B'
B' + A' ⟶ B'
D' + 1 . ⟶ D'
GOTO 1 1
END
B' / D' ⟶ B'
√ B' ⟶ B'
B' / C ⟶ C'
DPLY E B' C' D' DPLY
```

The following program can be used to calculate the gain of an amplifier stage by analyzing the output as stored in a display array of the Norland PCO consisting of at least ten cycles of sine wave.

```
0 . ⟶ A'
0 . ⟶ B'
0 . ⟶ C'
1 0 . ⟶ D
D IF> ⟶ A'
PMAX
COOR
B + V ⟶ B
D - 1 . ⟶ D
GOTO 5
END
B / 1 0 . ⟶ B
```

```
1 0 . 0 ⟶ D
D F A'
PMIN'                    (blue key - PMIN)
COOR
C + V ⟶ C
D - 1 . 0 ⟶ D
GOTO 1 4
END
C / 1 0 . 0 ⟶ C
B - C ⟶ C
C / A ⟶ E
DPLY A C E DPLY
```

To run the program, the peak-to-peak amplitude is first entered into A. The P cursor is placed on the output waveform to be analyzed ahead of the first positive peak. A negative peak must be ahead of this position, and there must be at least ten peaks.

On noisy waveforms, the program might not run properly; it may include small intermediate peaks away from the true peaks in the averages.

# APPENDIX J

## INSTRUMENTS USED IN TESTS

| Type of Instrument | Manufacturer | Model Number | PI Number | Accuracy |
|---|---|---|---|---|
| Power supply 0-120 V dc 0-12 A, reg. | Sorenson | 1120S | Owned by Leasametrics | |
| Power supply, 0-50 V dc, 0-0.5 A, reg.dual | Power Designs | TW5005 | 40402 | 3% |
| Power supply, 0-50 V dc 0-0.5 A, reg.dual | Power Designs | TW5005 | 4146 | 3% |
| Power supply, 0-50 V dc, 0-1.5 A, reg. | Heathkit | IP-27 | 4623 | 3% |
| Power supply, 0-60 V dc, 0-4 A, reg. | Lambda | LK344A-FM | Govt. #NO1-HV-9-2253/2253-A5 | 3% |
| Multimeter | Simpson | 260-4 | 2010 | 3% |
| Multimeter | Simpson | 260-6M | 98535 | 3% |
| Multimeter | Triplett | 310-C | 4540 | 3% |
| x-y strip chart recorder, analog input | Houston Instruments | 2000 Omnigraphic | 1381 | 0.2% (linearity, 0.1%; repeatability, 0.1%; resettability, 0.05%; full scale in each case) |
| Function generator, 4 function, gateable, triggerable, with dc offset | IEC | F-74 | 40562 | frequency,2%, ±1% of meter setting |
| Programmable calculating oscilloscope | Norland | NI2001A | Govt owned | time base, 0.01% +1 LSB; aperture time, 2 ns; aperture jitter 0.2 ns typ. |

| Type of Instrument | Manufacturer | Model Number | TI Number | Accuracy |
|---|---|---|---|---|
| Plug in for PCO | Norland | NI2202 | Govt. owned | Voltage, ½% (full scale) +1 LSB; resolution, 8 binary bits |
| Plug in for PCO | do | do | do | do |
| Display screen for PCO | do | 1332A | do | -- |

# APPENDIX K

# THEORY OF VARIABLE LOAD

This appendix discusses the impacts of variation in load capacitance and the effects of nonlinear capacitance on amplifier performance. This subject is of interest because there is some evidence that the mirror actuators may present such a load.

The actuator amplifier uses resonant charging of the capacitive load. The resonant circuit consists of the load and $L_1$ (Figure 8). The period of resonance, for a load capacitance of 0.05 μf, is about 160 μs. The resonant period is inversely proportional to the square root of the load capacitance. The power switching period varies from 1 to 16 μs, that is, from 2.5 to 40 percent of a quarter period.

The predictor function of the control logic calculates the time the PS transistor must be left on for any given situation of initial stack voltage and required change; in general the time required is directly proportional to the load capacitance, or nearly so. By design, the time required to correctly change a 0.05 μf load capacitance is correctly calculated for all combinations of initial stack voltage and required change. However, because of various assumptions and approximations in the design, as well as inaccuracies in the values of components and unwanted and/or unanticipated side effects (e.g., capacitance within transistor junctions), there is some error in the time interval calculations even with the 0.05 μf load capacitance.

Whenever an error adds up to less than ± 10 percent, there is no problem, for the width of the dead band would absorb it. An error in the ±10 to 30 percent range is no real problem either, for in many cases the dead band still absorbs it, and in all

other cases a single extra clock cycle can effect a correction. The only noticeable signs present are a possible slight reduction of the slew rate, and a slight increase of swicching noise for certain types of signals.

Errors of greater than ±30 percent may cause some significant problems, and errors greater than ±50 percent are quite likely to do so. Over-timing will cause over-predicting, which will result in overshoots, an increase in switching noise, and possibly hunting. Under-timing will lower the slew rate and the large-signal frequency response.

Based on experience with the breadboard and prototype, the predicting errors of an operational actuator amplifier channel, optimized in detail design and properly tuned, can be expected to be less than 20 percent under any conditions, and roughly balanced between over-timing and under-timing.

When capacitive load of other than 0.05 μf is connected, the predicting errors will be those resulting from the overload or underload on top of those already present. Thus, a slight variation, ±10 per ent, should cause no undue problems, and variation of ±20 percent most probably will not.

Greater variations may cause significant problems. Under-loading of greater than 30 percent is likely to result in hunting and other symptoms of excessive switching noise. One possible option to avoid these problems would be to parallel the load with a padding capacitor, i.e., one selected so that its value plus the load equals roughly 0.05 μf. Another option would be to make the integrating capacitor $C_5$ in the predicting ramp (Figure 5) a variable trimmer. This would allow compensating for

an underload; it could be expected to do so for a value of load down to 40 percent of normal, below which the nonlinear capacitance of the zener diode might start to affect the ramp.

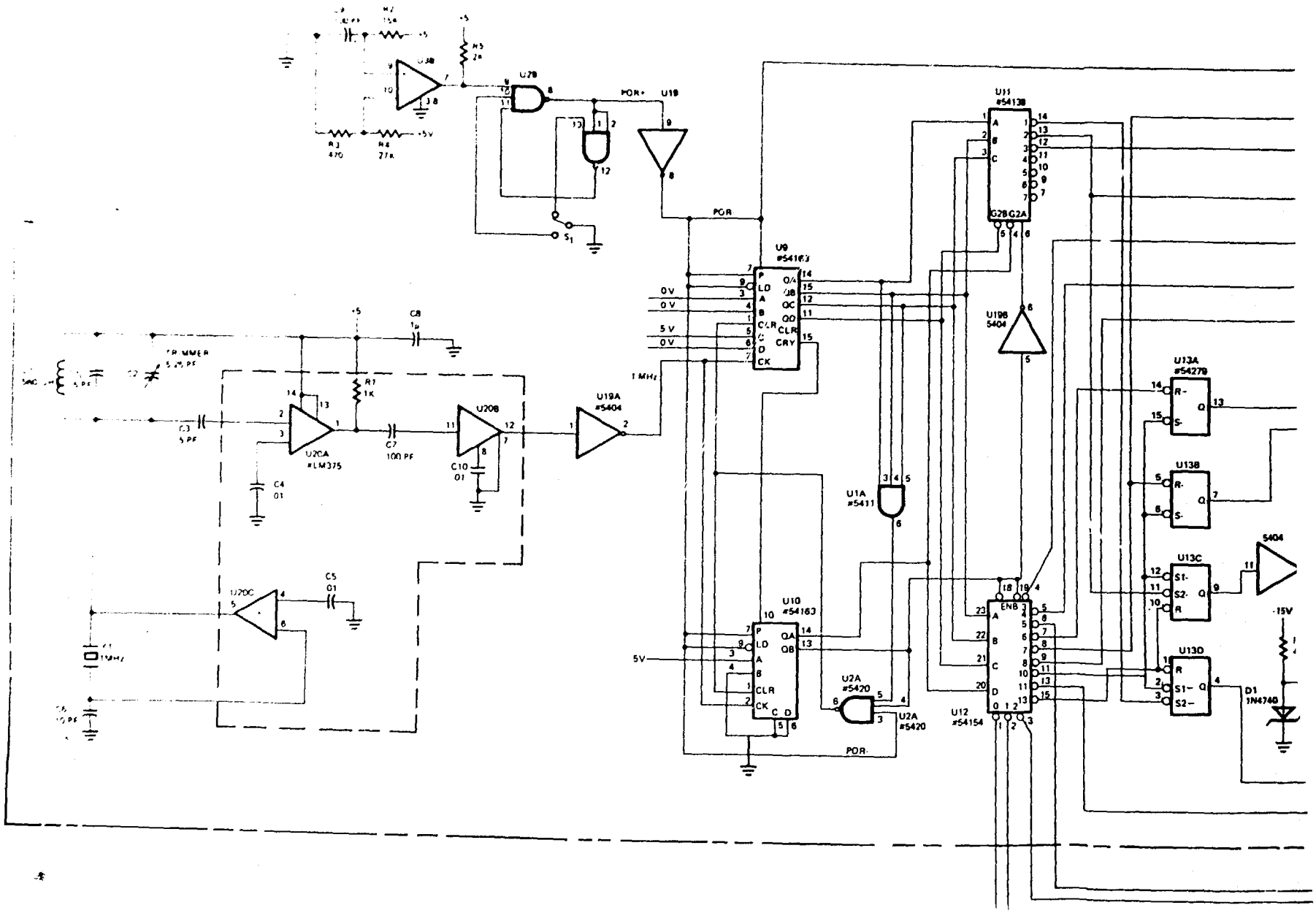
Overloading of greater than 30 percent may cause serious problems in that the transformer may saturate with high dc levels or a large amplitude step change. The slew rate and the large signal frequency response will decrease in inverse proportion to the overload. There are no easy options to compensate for this problem; it can be prevented only with a physically larger transformer, which is already the largest single component of the channel amplifier.

A nonlinear load capacitance is one in which the capacitance varies incrementally with voltage; this is also true where hysteresis is involved. However, the actuator amplifier works by effecting incremental changes in the load voltage. Thus a nonlinear load is one in which capacitance changes from one clock cycle to the next, but can be considered essentially constant during a clock cycle.

The effects of incremental undercapacitance or underloading are similar to those to be expected if the overall capacitance were low, except that this is most likely to occur at high dc voltage. Here the effect of overpredicting is likely to be compensated by the increased setback effect, i.e., the voltage fall-off on the load just after the HVG opens due to the charging of the internal capacitances of the transistors, diodes, etc. On the other hand, such options as padding capacitors and tuning trimmers are obviously not available on an incremental basis.

Incremental overcapacitance will result in reduced slew rate, as in the case of overall overcapacitance. Transformer saturation,

however, is not likely to be a problem, since overcapacitance is not likely to occur at high dc voltage. Saturation due to large steps would not be a problem either if the overcapacitance were present only over a small part of the total step commanded.


U2B
U2B
U19
POR+
POR
S1
U9
#54163
0V
0V
5V
0V
1 MHz
5V
U19A
#5404
U20B
U20A
#LM375
U20C
R7
1K
C8
1µ
C3
5 PF
C4
01
C7
100 PF
C10
01
C5
01
TRIMMER
5-45 PF
U1A
#5411
U2A
#5420
U2A
#5420
POR-
U10
#54163
U11
#54138
G2B G2A
U19B
5404
U12
#54154
ENB
U13A
#54279
U13B
U13C
U13D
5404
-15V
D1
1N4740

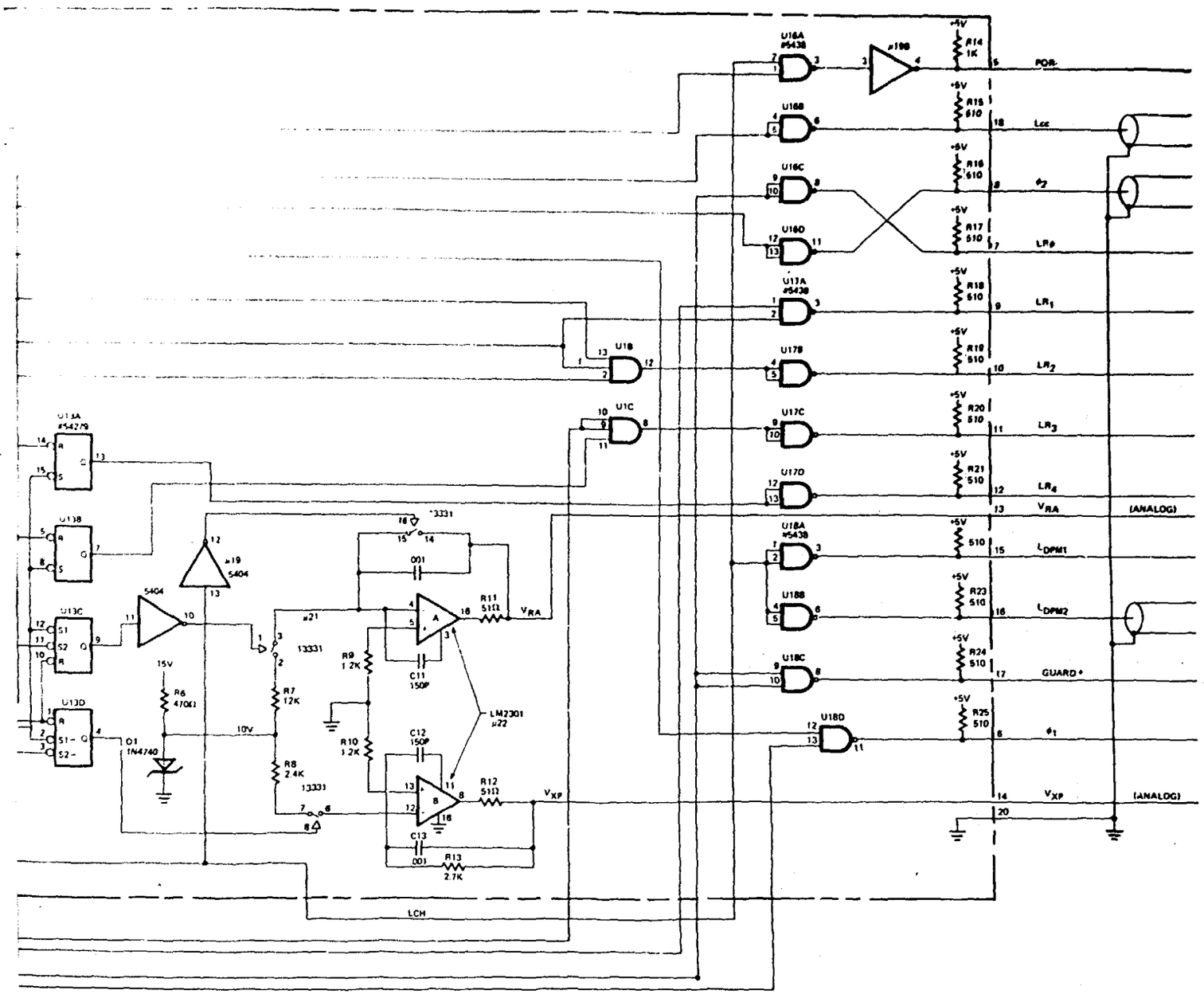



Figure 9. Common logic schematic.